Intel® Desktop Board D865PERL
Technical Product Specification

April 2003

Order Number: C31764-001

The Intel® Desktop Board D865PERL may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D865PERL Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D865PERL Technical Product Specification.	April 2003

This product specification applies to only the standard Intel Desktop Board D865PERL with BIOS identifier RL86510A.86A.

Changes to this specification will be published in the Intel Desktop Board D865PERL Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the Intel® Desktop Board D865PERL layout, components, connectors, power and environmental requirements, and BIOS. The TPS describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the Desktop Board and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the Desktop Board D865PERL
2	A map of the resources of the Desktop Board D865PERL
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions, which if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the Desktop Board D865PERL, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
GB	Gigabyte (1,073,741,824 bytes)
GB/sec	Gigabytes per second
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbits/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

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2 Technical Reference

3 Overview of BIOS Features

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1 Product Description

What This Chapter Contains

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the major features of the Intel® Desktop Board D865PERL.

Table 1. Feature Summary

Form Factor	ATX (12.0 inches by 9.6 inches [304.80 millimeters by 243.84 millimeters])
Processor	• Support for an Intel® Pentium® 4 processor in a mPGA478 socket with a 400/533/800 MHz system bus • Support for an Intel® Celeron® processor in a mPGA478 socket with a 400 MHz system bus
Memory	• Four 184-pin DDR SDRAM Dual Inline Memory Module (DIMM) sockets • Support for DDR 400, DDR 333, and DDR 266 • Support for up to 4 GB of system memory
Chipset	Intel® 865PE Chipset, consisting of: • Intel® 82865PE Memory Controller Hub (MCH) • Intel® 82801EB I/O Controller Hub (ICH5) or Intel® 82801ER I/O Controller Hub (ICH5-R) • Intel® 82802AB (4 Mbit) Firmware Hub (FWH)
Video	Universal 0.8/1.5 V AGP 3.0 connector (with integrated retention mechanism) supporting 1x, 4x, and 8x AGP cards
USB	Support for USB 2.0 devices
Peripheral Interfaces	• Eight USB ports • One serial port • One parallel port • Two Serial ATA interfaces • Two Parallel ATA IDE interfaces with UDMA 33, ATA-66/100 support • One diskette drive interface • PS/2* keyboard and mouse ports
Expansion Capabilities	Five PCI bus add-in card connectors
I/O Control	LPC Bus I/O controller
Hardware Monitor Subsystem	• Hardware monitoring and fan control ASIC • Voltage sense to detect out of range power supply voltages • Thermal sense to detect out of range thermal values • Four fan connectors • Four fan sense inputs used to monitor fan activity • Fan speed control

continued

Table 1. Feature Summary (continued)

BIOS	• Intel/AMI BIOS (resident in the Intel 82802AB FWH) • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS
Instantly Available PC Technology	• Support for PCI Local Bus Specification Revision 2.2 • Suspend to RAM support • Wake on PCI, RS-232, front panel, PS/2 devices, and USB ports

For information about	Refer to
The Desktop Board D865PERL's compliance level with ACPI, Plug and Play, and SMBIOS.	Section 1.4, page 17

1.1.2 Manufacturing Options

Table 2 describes the manufacturing options for the Desktop Board D865PERL. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

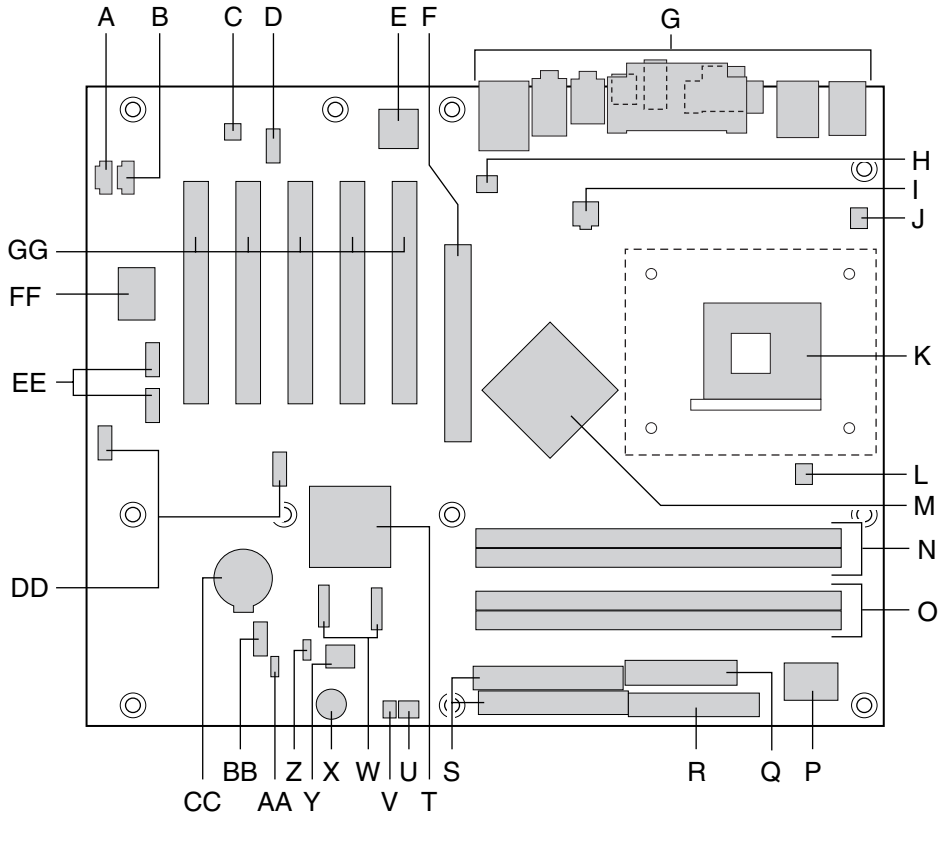
Table 2. Manufacturing Options

Audio	The board includes one of the following for AC '97 processing: • 6-channel audio subsystem using the Analog Devices AD1985 codec • Flex 6 audio subsystem using the Analog Devices AD1985 codec
LAN	The board includes one of the following: • 10/100 Mbits/sec LAN subsystem using the Intel® 82562EZ Platform LAN Connect (PLC) device • 10/100/1000 Mbits/sec LAN subsystem using the Intel® 82547EI PLC device
Intel RAID Technology	RAID 0 support on the two Serial ATA connectors implemented via the Intel 82801ER I/O Controller Hub (ICH5-R)
IEEE 1394a-2000 Interface	• Agere Systems FW323 Controller • Three IEEE 1394a-2000 ports

For information about	Refer to
Available configurations for the Desktop Board D865PERL	Section 1.2, page 16

1.1.3 Board Layout

Figure 1 shows the location of the major components on the Desktop Board D865PERL.



A	Auxiliary line input connector	R	Diskette drive connector
B	ATAPI CD-ROM connector	S	Parallel ATA IDE connectors
C	Audio codec	T	I/O Controller Hub (ICH5 or ICH5-R)
D	Front panel audio connector	U	Front chassis fan connector
E	Ethernet Platform LAN Connect device	V	Chassis intrusion connector
F	AGP connector	W	Serial ATA IDE connectors
G	Back panel connectors	X	Speaker
H	Rear chassis fan	Y	Intel 82802AB Firmware Hub (FWH)
I	+12 V power connector (ATX12V)	Z	BIOS setup configuration jumper
J	Voltage regulator fan	AA	Auxiliary front panel power LED
K	mPGA478 processor socket	BB	Front panel connector
L	Processor fan connector	CC	Battery
M	Intel 82865PE Memory Controller Hub (MCH)	DD	Front panel USB connectors
N	DIMM channel A	EE	IEEE 1394a-2000 front panel connectors (optional)
O	DIMM channel B	FF	IEEE 1394a-2000 controller (optional)
P	I/O controller	GG	PCI bus add-in card connectors
Q	Power connector		

Figure 1. Desktop Board D865PERL Components

1.1.4 Block Diagram

Figure 2 is a block diagram of the major functional areas of the Desktop Board D865PERL.

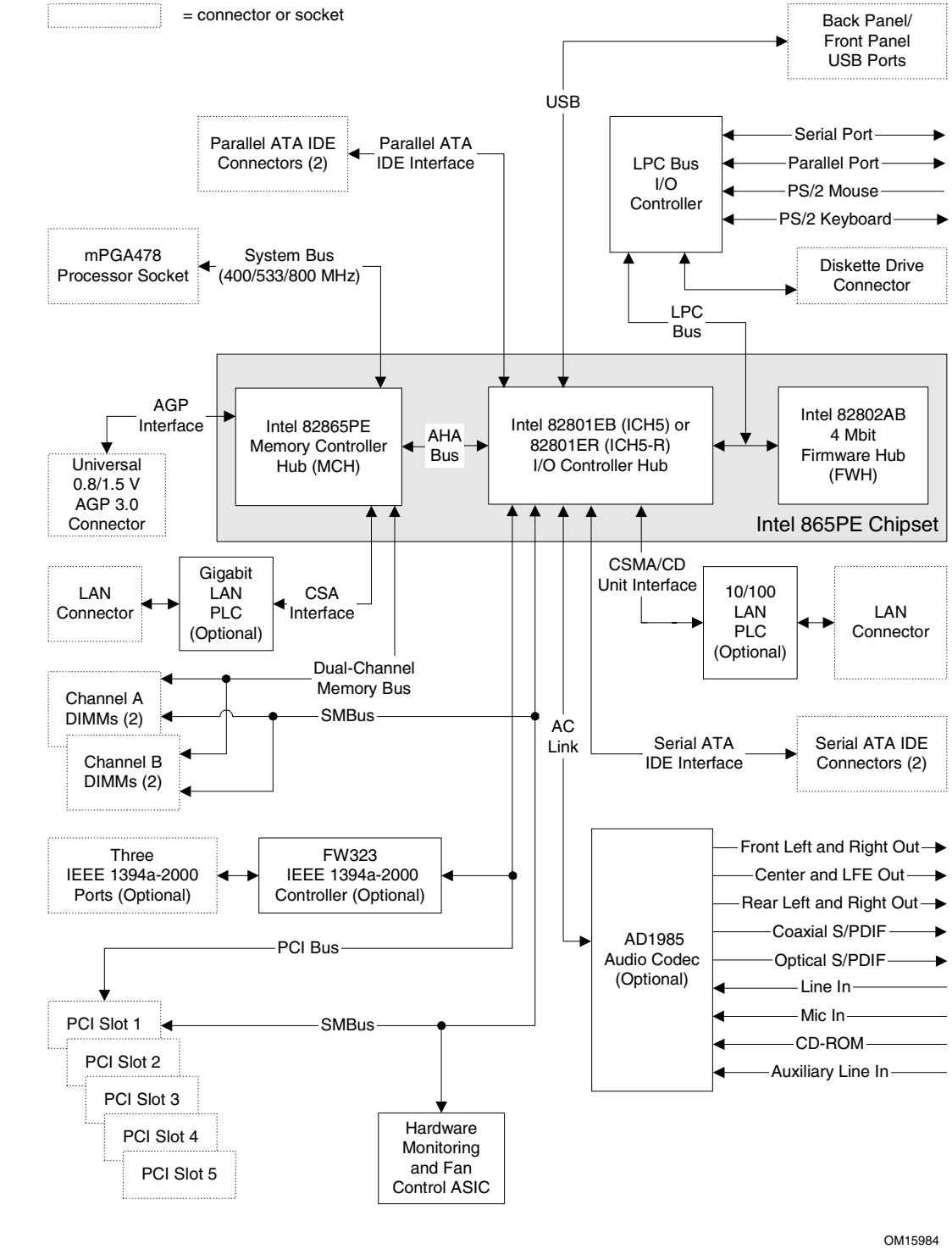


Figure 2. Block Diagram

1.2 Online Support

To find information about…	Visit this World Wide Web site:
The Desktop Board D865PERL, look under "Desktop Board Products" or "Desktop Board Support"	http://www.intel.com/design/motherbd http://support.intel.com/support/motherboards/desktop
Available configurations for the Desktop Board D865PERL	http://developer.intel.com/design/motherbd/rl/rl_available.htm
Processor data sheets	http://www.intel.com/design/litcentr
ICH5 addressing	http://developer.intel.com/design/chipsets/datashts
Custom splash screens	http://www.intel.com/design/motherbd/gen_indx.htm
Audio software and utilities	http://www.intel.com/design/motherbd
LAN software and drivers	http://www.intel.com/design/motherbd

1.3 Operating System Support

The Desktop Board D865PERL support drivers for onboard hardware and subsystems under the following operating systems:

- Microsoft Windows* XP
- Windows 2000
- Windows ME
- Windows 98 SE

✏ NOTES

- *IEEE 1394a-2000 support has been tested with Windows 2000 and Windows XP drivers and is not currently supported by any other operating system.*
- *RAID is supported only on Microsoft Windows XP.*
- *Native USB 2.0 support has been tested with drivers for Windows 2000 (with Service Pack 3) and Windows XP (with Service Pack 1) and is not currently supported by any other operating system in the list above. Check Intel's Desktop Board website for possible driver updates for other operating systems.*
- *Third party vendors may offer other drivers.*

For information about	Refer to
Supported drivers	Section 1.2, page 16

1.4 Design Specifications

Table 3 lists the specifications applicable to the Desktop Board D865PERL.

Table 3. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
1394	IEEE Std 1394-1995, *IEEE Standard for a High Performance Serial Bus*	November 8, 2001, Institute of Electrical and Electronic Engineers.	http://standards.ieee.org/catalog/olis/busarch.html
	IEEE Std 1394a-2000, *IEEE Standard for a High Performance Serial Bus – Amendment 1*	June 29, 2000, Institute of Electrical and Electronic Engineers.	http://standards.ieee.org/catalog/olis/busarch.html
AC '97	*Audio Codec '97*	Revision 2.2, September 2000, Intel Corporation.	ftp://download.intel.com/labs/media/audio/download/ac97r22.pdf
ACPI	*Advanced Configuration and Power Interface Specification*	Version 2.0a, March 31, 2002, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Limited, and Toshiba Corporation.	http://www.acpi.info/DOWNLOADS/ACPIspec-2-0a.pdf
AGP	*Accelerated Graphics Port Interface Specification*	Revision 3.0, September 1, 2002 Intel Corporation.	http://www.agpforum.org/specs_specs.htm
AMI BIOS	*AMIBIOS Desktop Core 8.0*	AMIBIOS 8.0, 2001, American Megatrends, Inc.	http://www.ami.com/support/doc/amibios8.pdf
ASF	*Alert Standard Format (ASF) Specification*	Version 1.03, June 20, 2001, DMTF, Intel Corporation.	http://www.dmtf.org/standards/documents/ASF/DSP0114.pdf
ATA/ ATAPI-5	*Information Technology-AT Attachment with Packet Interface - 5* (ATA/ATAPI-5)	Revision 3, February 29, 2000, Contact: T13 Chair, Seagate Technology.	http://www.t13.org
ATX	*ATX Specification*	Version 2.1, June 2002, Intel Corporation.	http://www.formfactors.org/developer/specs/atx/atx2_1.pdf
ATX12V	*ATX/ATX12V Power Supply Design Guide*	Version 1.2, August 2000, Intel Corporation.	http://www.formfactors.org/developer/specs/atx/atxspecs.htm

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
BIS	*Boot Integrity Services (BIS) Application Programming Interface (API)*	Version 1.0, August 4, 1999, Intel Corporation.	http://www.intel.com/labs/manage/wfm/wfmspecs.htm
DDR SDRAM	*Double Data Rate (DDR) SDRAM Specification*	Version 2.0, May 2002, JEDEC Solid State Technology Association.	http://www.jedec.org/
	Design Specification for a 184 Pin DDR Unbuffered DIMM	Revision 1.0, October 2001, JEDEC Solid State Technology Association.	http://www.jedec.org/
	Intel® JEDEC DDR 200/266 Unbuffered DIMM Specification Addendum	Revision 0.9, September 27, 2001, Intel Corporation.	http://developer.intel.com/technology/memory/index.htm
EHCI	*Enhanced Host Controller Interface Specification for Universal Serial Bus*	Revision 1.0, March 12, 2002, Intel Corporation.	http://developer.intel.com/technology/usb/download/ehci-r10.pdf
EPP	*IEEE Std 1284.1-1997* (Enhanced Parallel Port)	Version 1.7, 1997, Institute of Electrical and Electronic Engineers.	http://standards.ieee.org/reading/ieee/std_public/description/busarch/1284.1-1997_desc.html
El Torito	*Bootable CD-ROM Format Specification*	Version 1.0, January 25, 1995, Phoenix Technologies Limited and International Business Machines Corporation.	http://www.phoenix.com/resources/specs-cdrom.pdf
LPC	*Low Pin Count Interface Specification*	Revision 1.0, September 29, 1997, Intel Corporation.	http://www.intel.com/design/chipsets/industry/lpc.htm
OHCI	*OpenHCI – Open Host Controller Interface Specification for USB*	Release 1.0a, October 10, 1996, Compaq Computer Corp., Microsoft Corporation, and National Semiconductor Corp.	http://h18000.www1.hp.com/productinfo/development/openhci.html
PCI	*PCI Local Bus Specification*	Revision 2.2, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/specifications
	PCI Bus Power Management Interface Specification	Revision 1.1, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/specifications

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
Plug and Play	*Plug and Play BIOS Specification*	Version 1.0a, May 5, 1994, Compaq Computer Corporation, Phoenix Technologies Limited, and Intel Corporation.	http://www.microsoft.com/hwdev/tech/PnP/default.asp
PXE	*Preboot Execution Environment*	Version 2.1, September 20, 1999, Intel Corporation.	ftp://download.intel.com/labs/manage/wfm/download/pxespec.pdf
Serial ATA (SATA)	*Serial ATA: High Speed Serialized AT Attachment*	Revision 1.0, August 29, 2001, APT Technologies, Inc., Dell Computer Corporation, IBM Corporation, Intel Corporation, Maxtor Corporation, and Seagate Technology.	http://www.serialata.com/
SMBIOS	*System Management BIOS*	Version 2.3.1, March 16, 1999, American Megatrends Incorporated, Award Software International Incorporated, Compaq Computer Corporation, Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, and SystemSoft Corporation.	http://www.dmtf.org/download/standards/DSP0119.pdf
UHCI	*Universal Host Controller Interface Design Guide*	Revision 1.1, March 1996, Intel Corporation.	http://developer.intel.com/design/USB/UHCI11D.htm
USB	*Universal Serial Bus Specification*	Revision 2.0, April 27, 2000, Compaq Computer Corporation, Hewlett-Packard Company, Lucent Technologies Inc., Intel Corporation, Microsoft Corporation, NEC Corporation, and Koninklijke Philips Electronics N.V.	http://www.usb.org/developers/docs.html
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation.	http://www.intel.com/labs/manage/wfm/wfmspecs.htm

1.5 Processor

NOTE

Refer to Thermal Considerations (Section 2.12, page 80) for important information when using an Intel Pentium 4 processor operating above 2.80 GHz with this Intel desktop board.

The board is designed to support the following:

- Intel Pentium 4 processors in an mPGA478 processor socket with a 400/533/800 MHz system bus
- Intel Celeron processors with a 400 MHz system bus

See the Intel web site listed below for the most up-to-date list of supported processors.

For information about…	Refer to:
Supported processors for the D865PERL board	http://www.intel.com/design/motherbd/rl/rl_proc.htm

CAUTION

Use only the processors listed on web site above. Use of unsupported processors can damage the board, the processor, and the power supply.

INTEGRATOR'S NOTES

- *Use only ATX12V-compliant power supplies with the board. ATX12V power supplies have an additional power lead that provides required supplemental power for the processor. Always connect the 20-pin and 4-pin leads of ATX12V power supply to the corresponding connectors, otherwise the board will not boot.*
- *Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.*
- *Refer to Table 4 on page 21 for a list of supported system bus frequency and memory speed combinations.*

For information about	Refer to
Power supply connectors	Section 2.8.2.2, page 63

1.6 System Memory

1.6.1 Memory Features

The Desktop Board D865PERL has four DIMM sockets and supports the following memory features:

- 2.5 V (only) 184-pin DDR SDRAM DIMMs with gold-plated contacts
- Unbuffered, single-sided or double-sided DIMMs with the following restriction:

  Double-sided DIMMS with x16 organization are not supported.
- 4 GB maximum total system memory. Refer to Section 2.2.1 on page 51 for information on the total amount of addressable memory.
- Minimum total system memory: 64 MB
- Non-ECC DIMMs
- Serial Presence Detect
- DDR400, DDR333, and DDR266 SDRAM DIMMs

Table 4 lists the supported system bus frequency and memory speed combinations.

Table 4. Supported System Bus Frequency and Memory Speed Combinations

To use this type of DIMM…	The processor's system bus frequency must be…
DDR400	800 MHz
DDR333	800 or 533 MHz (Note)
DDR266	800, 533, or 400 MHz

Note: When using an 800 MHz system bus frequency processor, DDR333 memory is clocked at 320 MHz. This minimizes system latencies to optimize system throughput.

NOTES

- *Remove the AGP video card before installing or upgrading memory to avoid interference with the memory retention mechanism.*
- *To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.*

For information about	Refer to
Obtaining DDR SDRAM specifications	Section 1.4, page 17

Table 5 lists the supported DIMM configurations.

Table 5. Supported Memory Configurations

DIMM Capacity	Configuration	DDR SDRAM Density	DDR SDRAM Organization Front-side/Back-side	Number of DDR SDRAM Devices
64 MB	SS	64 Mbit	8 M x 8/empty	8
64 MB	SS	128 Mbit	8 M x 16/empty	4
128 MB	DS	64 Mbit	8 M x 8/8 M x 8	16
128 MB	SS	128 Mbit	16 M x 8/empty	8
128 MB	SS	256 Mbit	16 M x 16/empty	4
256 MB	DS	128 Mbit	16 M x 8/16 M x 8	16
256 MB	SS	256 Mbit	32 M x 8/empty	8
256 MB	SS	512 Mbit	32 M x 16/empty	4
512 MB	DS	256 Mbit	32 M x 8/32 M x 8	16
512 MB	SS	512 Mbit	64 M x 8/empty	8
1024 MB	DS	512 Mbit	64 M x 8/64 M x 8	16

Note: In the second column, “DS” refers to double-sided memory modules (containing two rows of DDR SDRAM) and “SS” refers to single-sided memory modules (containing one row of DDR SDRAM).

1.6.2 Memory Configurations

The Intel 82865PE MCH component provides two features for enhancing memory throughput:

- Dual Channel memory interface. The board has two memory channels, each with two DIMM sockets, as shown in Figure 3
- Dynamic Addressing Mode. Dynamic mode minimizes overhead by reducing memory accesses

Table 6 summarizes the characteristics of Dual and Single Channel configurations with and without the use of Dynamic Mode.

Table 6. Characteristics of Dual/Single Channel Configuration with/without Dynamic Mode

Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched (Example configurations are shown in Figure 4)
	Dual Channel without Dynamic Mode	• DIMMs matched from Channel A to Channel B • DIMMs not matched within channels (Example configuration is shown in Figure 5)
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel (Example configurations are shown in Figure 6)
Lowest	Single Channel without Dynamic Mode	DIMMs not matched (Example configurations are shown in Figure 7)

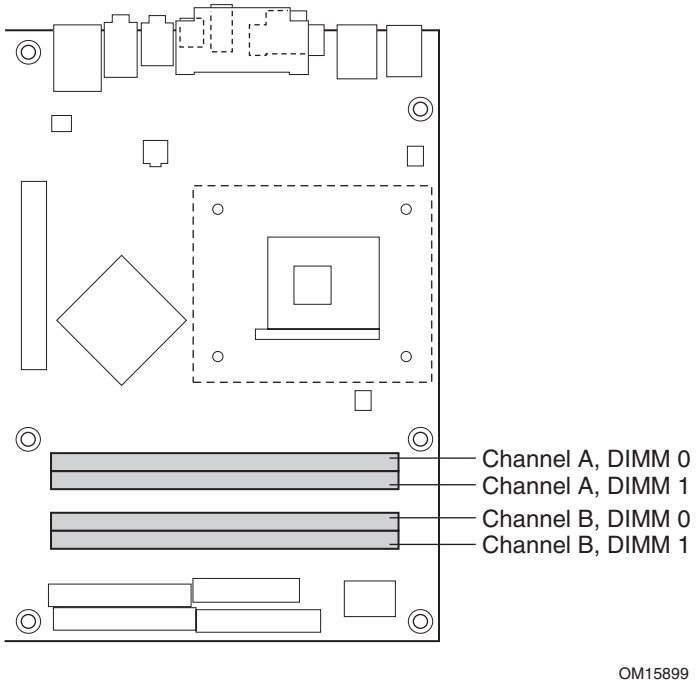
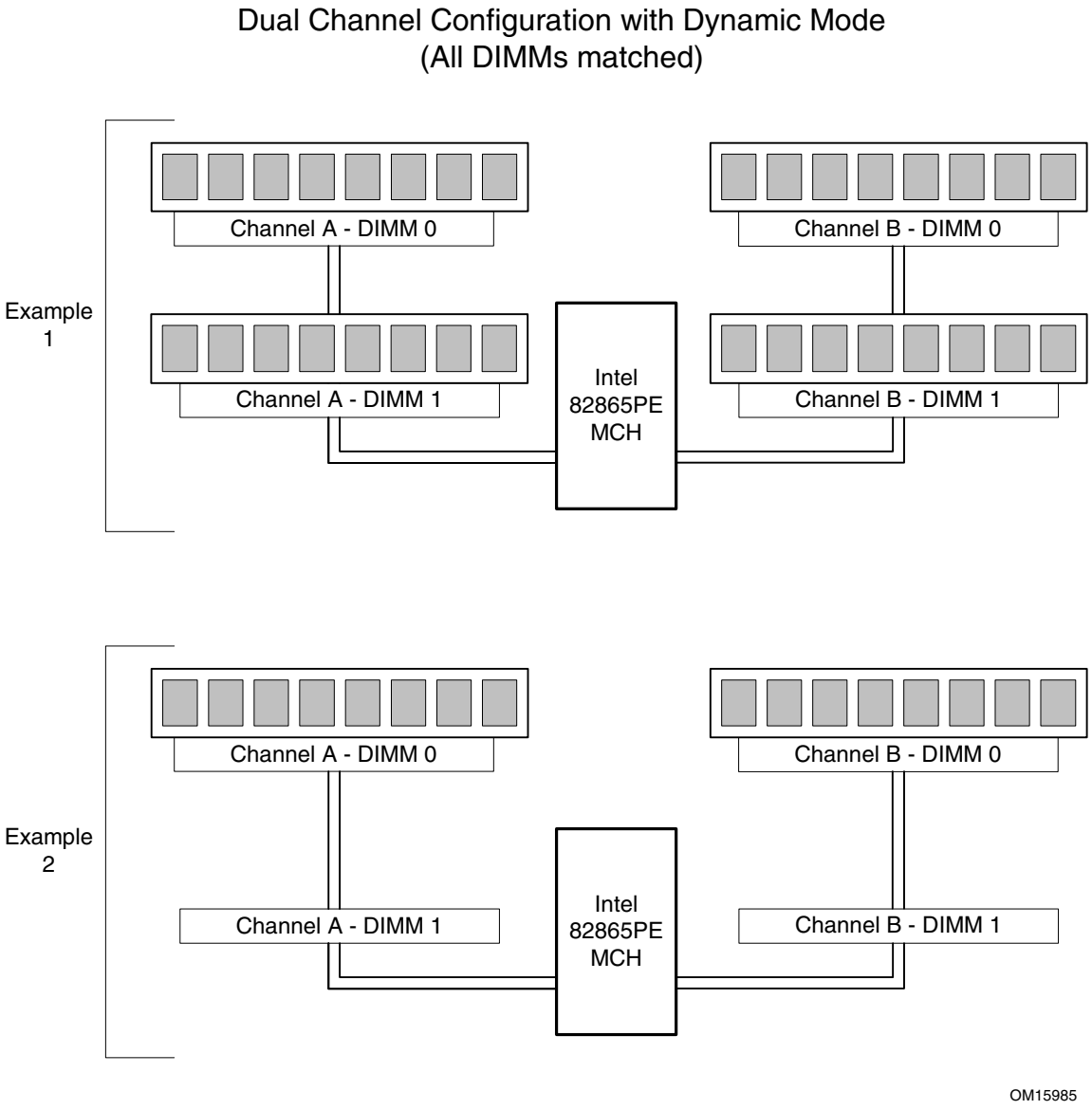


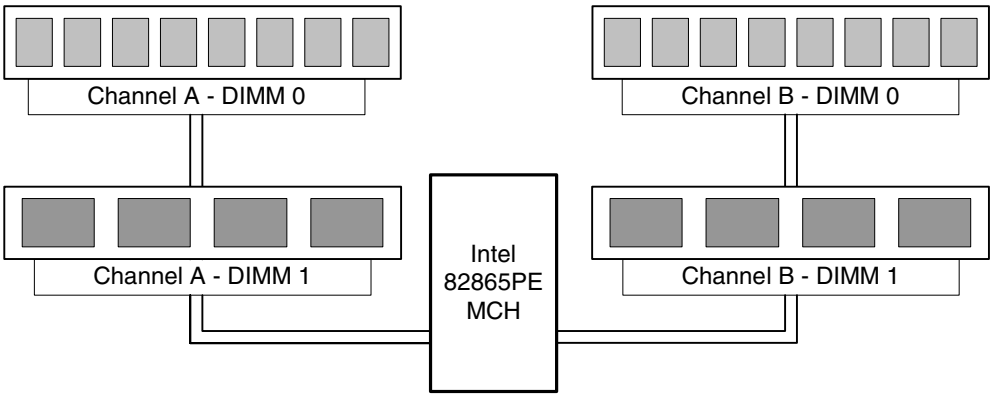
Figure 3. Memory Channel Configuration



Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched
	Dual Channel without Dynamic Mode	• DIMMs matched from Channel A to Channel B • DIMMs not matched within channels
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Figure 4. Examples of Dual Channel Configuration with Dynamic Mode

Dual Channel Configuration without Dynamic Mode
- DIMMs not matched within channel
- DIMMs match Channel A to Channel B



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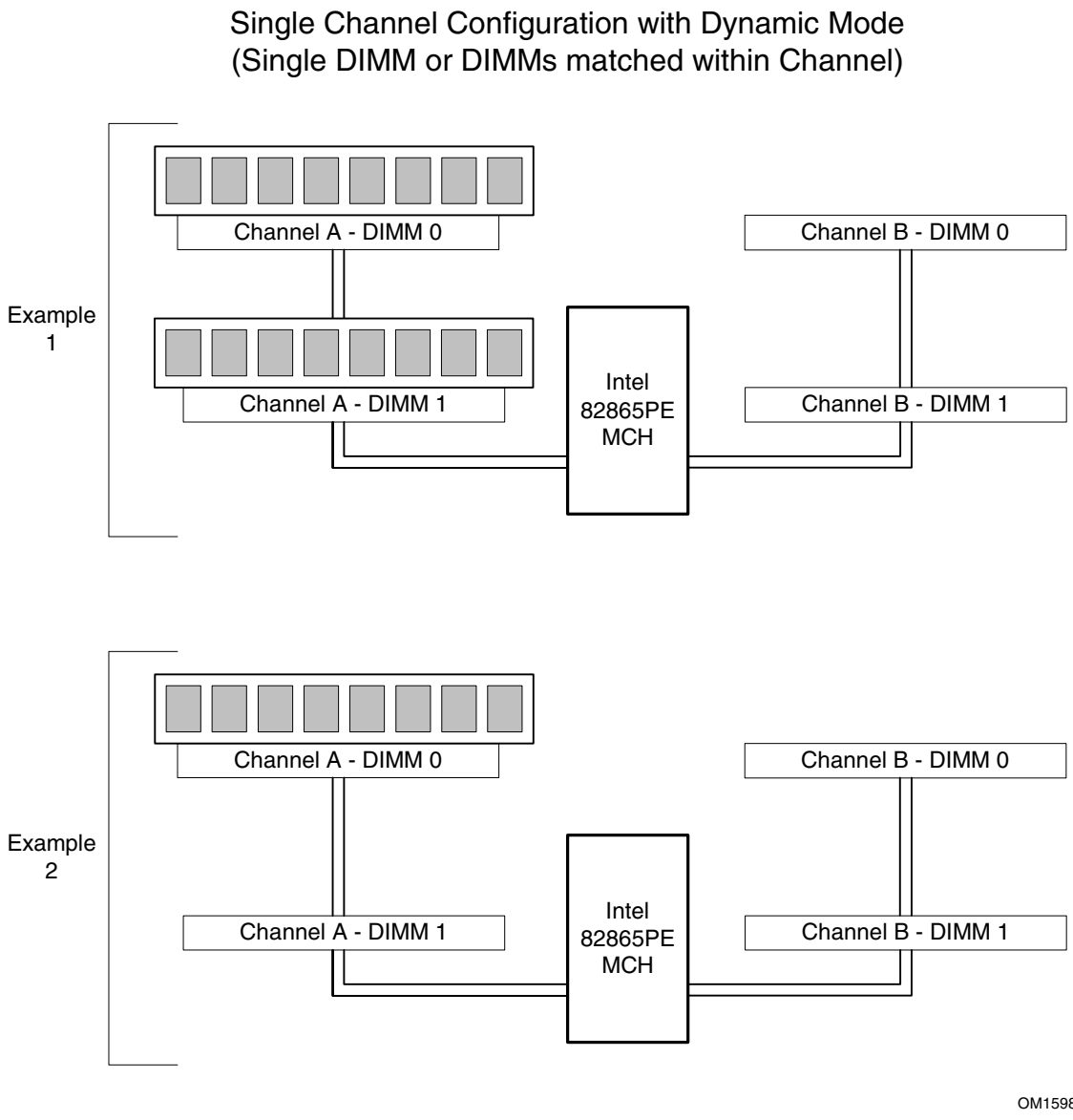
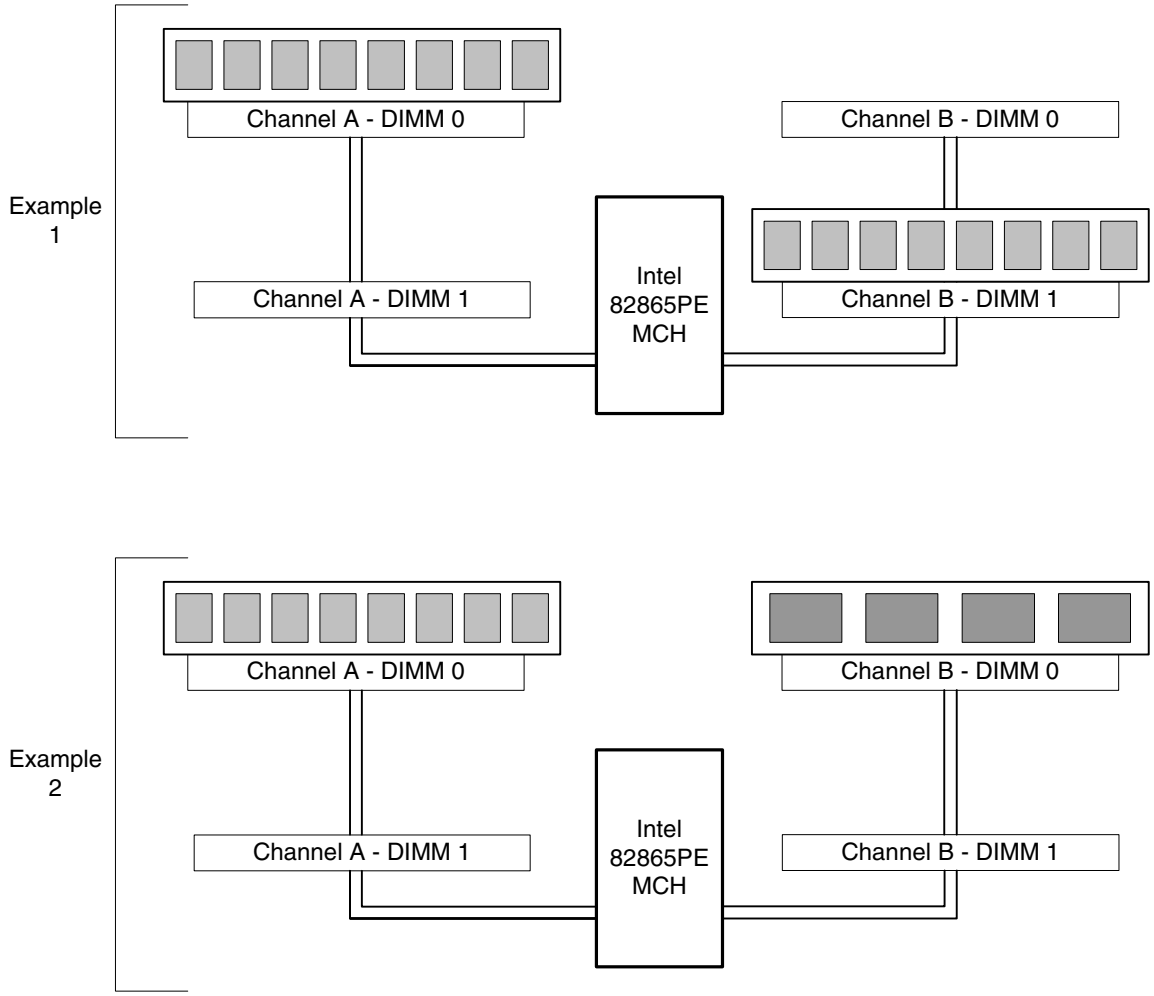
Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched
⇧	Dual Channel without Dynamic Mode	• DIMMs matched from Channel A to Channel B • DIMMs not matched within channels
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Figure 5. Example of Dual Channel Configuration without Dynamic Mode



Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched
	Dual Channel without Dynamic Mode	• DIMMs matched from Channel A to Channel B • DIMMs not matched within channels
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Figure 6. Examples of Single Channel Configuration with Dynamic Mode



Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched
	Dual Channel without Dynamic Mode	• DIMMs matched from Channel A to Channel B • DIMMs not matched within channels
	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Figure 7. Examples of Single Channel Configuration without Dynamic Mode

1.7 Intel® 865PE Chipset

The Intel 865PE chipset consists of the following devices:

- Intel 82865PE Memory Controller Hub (MCH) with Accelerated Hub Architecture (AHA) bus
- Intel 82801EB I/O Controller Hub (ICH5) with AHA bus or Intel 82801ER I/O Controller HUB (ICH5-R)
- Intel 82802AB (4 Mbit) Firmware Hub (FWH)

The MCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the Accelerated Hub Architecture interface. The ICH5 is a centralized controller for the Desktop Board D865PERL's I/O paths. The FWH provides the nonvolatile storage of the BIOS. The component combination provides the chipset interfaces as shown in Figure 8.

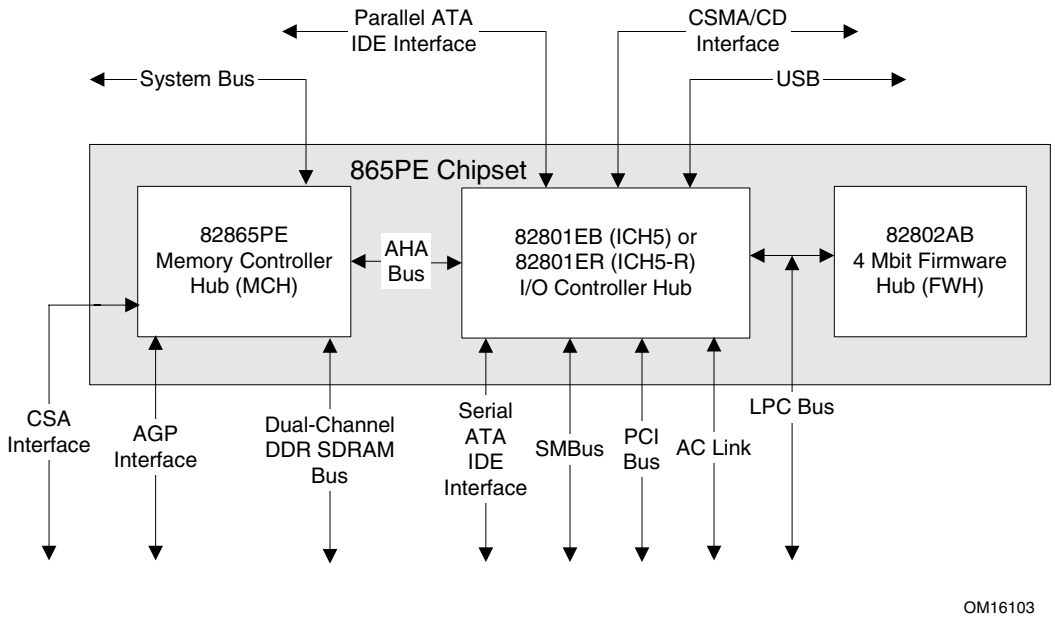


Figure 8. Intel 865PE Chipset Block Diagram

For information about	Refer to
The Intel 865PE chipset	http://developer.intel.com
Resources used by the chipset	Chapter 2

1.7.1 AGP

The AGP connector supports the following:

- 4x, 8x AGP 3.0 add-in cards with 0.8 V I/O
- 1x, 4x AGP 2.0 add-in cards with 1.5 V I/O

AGP is a high-performance interface for graphics-intensive applications, such as 3D applications. While based on the *PCI Local Bus Specification*, Rev. 2.2, AGP is independent of the PCI bus and

is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amounts of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent efficiency

INTEGRATOR'S NOTES

- *AGP 2x operation is not supported.*
- *Install memory in the DIMM sockets prior to installing the AGP video card to avoid interference with the memory retention mechanism.*
- *The AGP connector is keyed for Universal 0.8 V AGP 3.0 specification-compatible cards or 1.5 V AGP 2.0 specification-compatible cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.*

For information about	Refer to
The location of the AGP connector	Figure 1, page 14
Obtaining the *Accelerated Graphics Port Interface Specification*	Section 1.4, page 17

1.7.2 USB

The Desktop Board D865PERL supports up to eight USB 2.0 ports, supports UHCI and EHCI, and uses UHCI- and EHCI-compatible drivers.

The ICH5/ICH5-R provides the USB controller for all ports. The port arrangement is as follows:

- Two ports are implemented with stacked back panel connectors, adjacent to the PS/2 connectors
- Two ports are implemented with stacked back panel connectors, adjacent to the audio connectors
- Four ports are routed to two front panel USB connectors

NOTES

- *Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.*
- *Native USB 2.0 support has been tested with drivers for Windows 2000 (with Service Pack 3) and Windows XP (with Service Pack 1) and is not currently supported by any other operating system. Check Intel's Desktop Board website for possible driver updates for other operating systems.*

For information about	Refer to
The location of the USB connectors on the back panel	Figure 19, page 60
The location of the front panel USB connectors	Figure 23, page 70
The signal names of the front panel USB connector	Figure 25, page 73
The front panel, EHCI, UHCI, and USB specifications	Section 1.4, page 17

1.7.3 IDE Support

The board provides four IDE interface connectors:

- Two Parallel ATA IDE connectors, which support a total of four devices (two per connector)
- Two Serial ATA IDE connectors, which support one drive per connector

1.7.3.1 Parallel ATA IDE Interfaces

The ICH5's Parallel ATA IDE controller has two independent bus-mastering Parallel ATA IDE interfaces that can be independently enabled. The Parallel ATA IDE interfaces support the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH5's ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The Parallel ATA IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes listed in Section 4.4.4.1 on page 105.

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The Desktop Board D865PERL supports Laser Servo (LS-120) diskette technology through the Parallel ATA IDE interfaces. The BIOS supports booting from an LS-120 drive.

NOTE

The BIOS will always recognize an LS-120 drive as an ATAPI floppy drive. To ensure correct operation, do not configure the drive as a hard disk drive.

For information about	Refer to
The location of the Parallel ATA IDE connectors	Figure 22, page 68

1.7.3.2 Serial ATA Interfaces

The ICH5's Serial ATA controller offers two independent Serial ATA ports with a theoretical maximum transfer rate of 150 MB/s per port. One device can be installed on each port for a maximum of two Serial ATA devices. A point-to-point interface is used for host to device connections, unlike IDE which supports a master/slave configuration and two devices per channel.

For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard

IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI resource steering is used. Native mode is the preferred mode for configurations using the Windows XP and Windows 2000 operating systems.

✎ NOTE

Many Serial ATA drives use new low-voltage power connectors and require adaptors or power supplies equipped with low-voltage power connectors.

For information about	Refer to
Serial ATA	http://www.serialata.org

1.7.3.3 Intel® RAID Technology

Boards equipped with the ICH5-R support RAID (Redundant Array of Independent Drives) level 0 on the Serial ATA ports. RAID 0 provides the ability to support striping. Two physical drives, of identical size, can be teamed together to create one logical drive. As data is written or retrieved from the logical drive, both drives operate in parallel, thus increasing the throughput.

✎ NOTE

The ICH5-R provides support for RAID 0 and RAID boot in Windows XP only.

1.7.3.4 RAID Boot Configuration Overview

A RAID array can be created by using the existing Serial ATA Ports, correctly configuring the BIOS, and installing drivers. The following steps are required to successfully establish a RAID configuration.

1. Enable RAID Support in BIOS.
2. Create a RAID array using the Intel® Application Accelerator (IAA) utility.
3. Install the IAA 3.0 RAID driver.
4. Format the RAID array.
5. Install the IAA 3.0 Companion Utility (this step is optional).

For information about	Refer to
The location of the Serial ATA connectors	Figure 22, page 68
The signal names of the Serial ATA connectors	Table 36, page 69
The BIOS Setup program's Boot menu	Table 73, page 118
Serial ATA RAID configuration	http://developer.intel.com/design/motherbd/rl/index.htm

1.7.4 Real-Time Clock, CMOS SRAM, and Battery

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

1.7.5 Intel® 82802AB Firmware Hub (FWH)

The 4 Mbit FWH provides the following:

- System BIOS program
- Logic that enables protection for storing and updating of platform information

1.8 I/O Controller

The I/O controller provides the following features:

- One serial port
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.2 MB or 1.44 MB diskette drive
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
SMSC LPC47M172 I/O controller	http://www.smsc.com
National Semiconductor PC87372 I/O Controller	http://www.national.com

1.8.1 Serial Port

The board has one serial port connector located on the back panel. The serial port supports data transfers at speeds up to 115.2 kbits/sec with BIOS support.

For information about	Refer to
The location of the serial port connector	Figure 19, page 60

1.8.2 Parallel Port

The 25-pin D-Sub parallel port connector is located on the back panel. Use the BIOS Setup program to set the parallel port mode.

For information about	Refer to
The location of the parallel port connector	Figure 19, page 60
Setting the parallel port's mode	Table 59, page 101

1.8.3 Diskette Drive Controller

The I/O controller supports one diskette drive. Use the BIOS Setup program to configure the diskette drive interface.

For information about	Refer to
The location of the diskette drive connector	Figure 22, page 68
The supported diskette drive capacities and sizes	Table 62, page 107

1.8.4 Keyboard and Mouse Interface

The PS/2 keyboard and mouse connectors are located on the back panel.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 19, page 60

1.9 IEEE 1394a-2000 Controller (Optional)

The Agere Systems FW323 PCI bus-based controller provides IEEE 1394a-2000 OHCI link and PHY core functionality. The controller supports:

- IEEE 1394a-2000-compliant or IEEE 1394-1995-compliant peripheral devices
- Isochronous and asynchronous data transfer
- Data transfer up to 400 Mbits/sec
- Peripheral hot swapping
- Plug and play

The Desktop Board D865PERL has one back panel and two front panel IEEE 1394a-2000 connectors.

NOTE

IEEE 1394a-2000 support has been tested with Windows 2000 and Windows XP drivers and is not currently supported by any other operating system.

For information about	Refer to
The location of the back panel IEEE 1394a-2000 connector	Figure 19, page 60
The location of the front panel IEEE 1394a-2000 connectors	Figure 23, page 70
The signal names of the front panel IEEE 1394a-2000 connectors	Figure 26, page 73
Obtaining IEEE standards: • 1394-1995, *IEEE Standard for a High Performance Serial Bus* • 1394a-2000, *IEEE Standard for a High Performance Serial Bus – Amendment 1*	Table 3, page 17

1.10 Audio Subsystem

The Desktop Board D865PERL includes one of the following:

- 6-channel audio subsystem based on the Analog Devices AD1985 codec (described on page 34)
- Flex 6 audio subsystem based on the Analog Devices AD1985 codec (described on page 36)

Both audio subsystems feature:

- Advanced jack sense with Auto Topology Switching that enables the audio codec to recognize what device is connected to an audio port and alerts the user if the wrong type of device has been connected
- Split digital/analog architecture for improved S/N (signal-to-noise) ratio: > 94 dB
- Power management support for ACPI 2.0 (driver dependent)

1.10.1 6-Channel Audio Subsystem (Optional)

The audio subsystem includes the following:

- Intel 82801EB I/O Controller Hub (ICH5)
- Analog Devices AD1985 audio codec
- Microphone input that supports either of the following:
  - A single dynamic, condenser, or electret microphone
  - Dual microphones for use with voice recognition software

The subsystem includes the following connectors.

- Front panel analog audio connector that can be used as a connector for routing the following signals to the front panel or used as a jumper block for routing the signals to the back panel (see page 74 for more information). The connector/jumper block includes pins for:
  - Front left and right out
  - Mic in
- Back panel analog audio connectors:
  - Front left and right out
  - Center and Low Frequency Effects (LFE) out
  - Rear left and right out
  - Line in
  - Mic in
- Back panel coaxial S/PDIF (RCA) connector
- Back panel optical S/PDIF (Toslink) connector
- ATAPI-style CD-ROM connector

NOTE

Powered speakers are required.

Figure 9 shows the back panel audio connectors for the 6-channel audio subsystem.

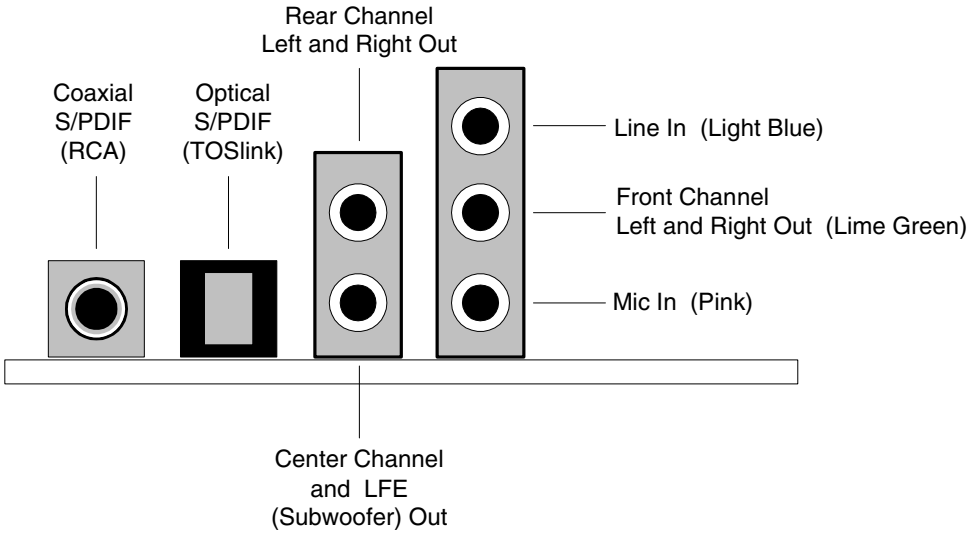


Figure 9. Back Panel Connectors for 6-Channel Audio Subsystem

Figure 10 is a block diagram of the 6-channel audio subsystem.

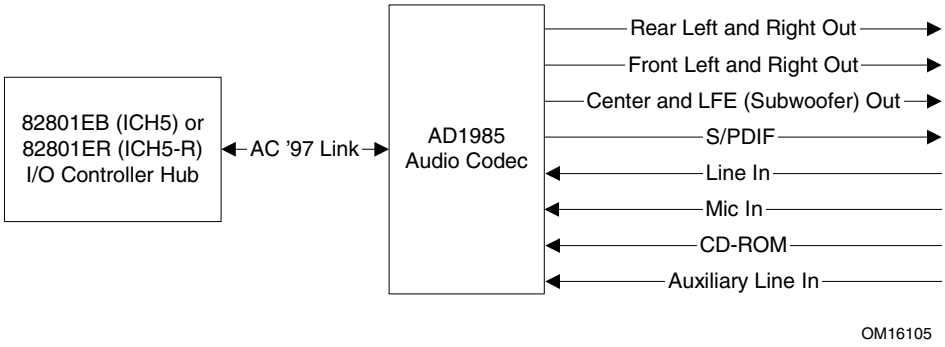


Figure 10. 6-Channel Audio Subsystem Block Diagram

For information about	Refer to
The front panel audio connector	Section 2.8.3, page 70
The back panel audio connectors	Section 2.8.1, page 60

1.10.2 Intel® Flex 6 Audio Subsystem (Optional)

The Flex 6 audio subsystem includes the following:

- Intel 82801EB I/O Controller Hub (ICH5)
- Analog Devices AD1985 audio codec
- Microphone input that supports a single dynamic, condenser, or electret microphone

The subsystem has the following connectors:

- ATAPI-style CD-ROM connector
- Front panel audio connector, including pins for:
  - Front left and right out
  - Mic in
- Back panel audio connectors that are configurable through the audio devices drivers. The available configurations are shown in Figure 11.

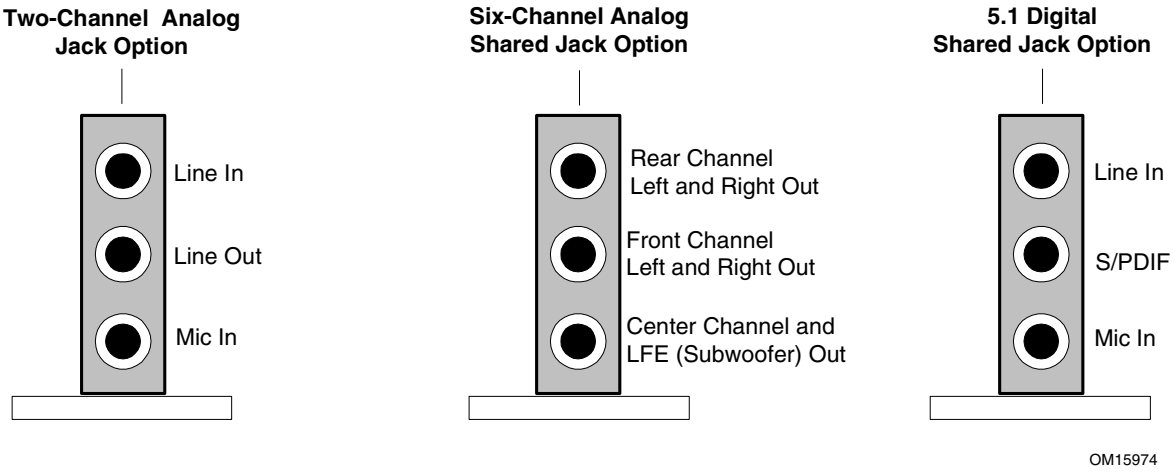


Figure 11. Back Panel Audio Connector Options for Flex 6 Audio Subsystem

INTEGRATOR'S NOTE

To access the S/PDIF signal with the 5.1 Digital Shared Jack option, connect an 1/8-inch stereo phone plug to RCA jack adapter/splitter as shown in Figure 12.

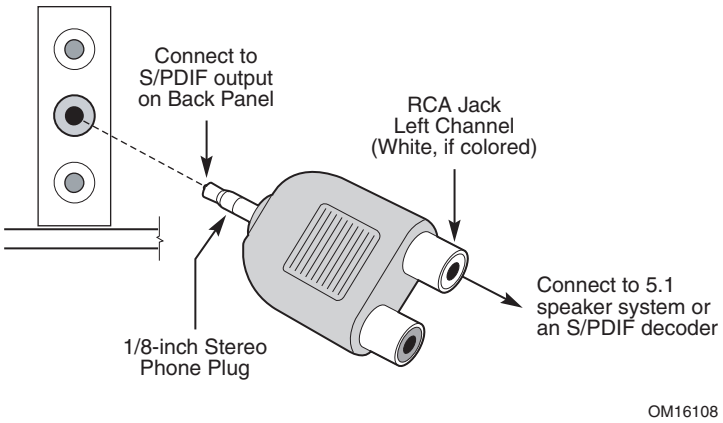


Figure 12. Adapter for S/PDIF Back Panel Connector

Figure 13 is a block diagram of the Flex 6 audio subsystem.

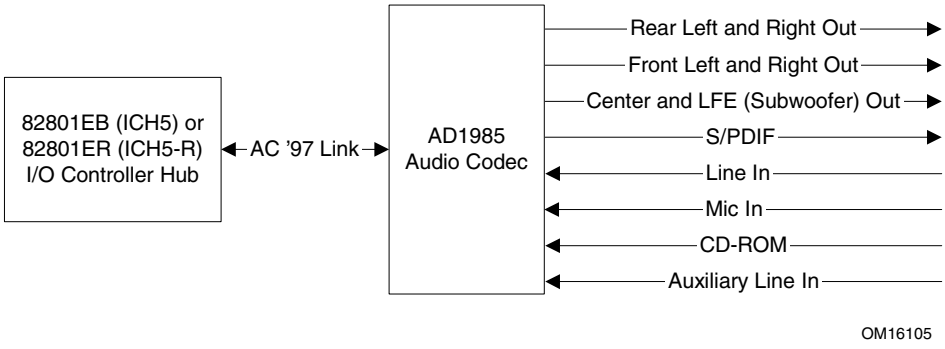


Figure 13. Flex 6 Audio Subsystem Block Diagram

For information about	Refer to
The front panel audio connector	Section 2.8.3, page 70
The back panel audio connectors	Section 2.8.1, page 60

1.10.3 Audio Connectors

1.10.3.1 Auxiliary Line In Connector

A 1 x 4-pin ATAPI-style connector connects the left and right channel signals of an internal audio device to the audio subsystem.

For information about	Refer to
The location of the optional auxiliary line in connector	Figure 20, page 63
The signal names of the optional auxiliary line in connector	Table 26, page 64

1.10.3.2 Front Panel Audio Connector

A 2 x 5-pin connector provides mic in and line out signals for front panel audio connectors.

For information about	Refer to
The location of the connector	Section 2.8.3, page 70
The signal names of the front panel audio connector	Table 28, page 64

NOTE

The front panel audio connector is alternately used as a jumper block for routing audio signals. Refer to Section 2.9.1 on page 74 for more information.

1.10.3.3 ATAPI-Style CD-ROM Connector

A 1 x 4-pin connector connects an internal ATAPI CD-ROM drive to the audio mixer.

For information about	Refer to
The location of the ATAPI-style CD-ROM connector	Figure 22, page 68
The signal names of the ATAPI-style CD-ROM connector	Table 27, page 64

1.10.4 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining audio software and drivers	Section 1.2, page 16

1.11 LAN Subsystem

The LAN subsystem consists of the following:

- Physical layer interface device. As a manufacturing option, the board includes one of the following Platform LAN Connect (PLC) devices:
  - — Intel 82562EZ PLC for 10/100 Mbits/sec Ethernet LAN connectivity
  - — Intel 82547EI PLC for Gigabit (10/100/1000 Mbits/sec) Ethernet LAN connectivity
- RJ-45 LAN connector with integrated status LEDs

Additional features of the LAN subsystem include:

- PCI bus master interface
- CSMA/CD protocol engine
- Serial CSMA/CD unit interface that supports the 82562EZ
- 8-bit CSA port interface that support the 82547EI
- PCI power management
  - — Supports ACPI technology
  - — Supports LAN wake capabilities

1.11.1 10/100 Mbits/sec LAN Subsystem

The 10/100 Mbits/sec LAN subsystem includes the ICH5 (with its CSMA/CD interface), the Intel 82562EZ PLC, and an RJ-45 LAN connector with integrated status LEDs

1.11.1.1 Intel® 82562EZ Physical Layer Interface Device

The Intel 82562EZ provides the following functions:

- Basic 10/100 Ethernet LAN connectivity
- Full device driver compatibility
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

1.11.1.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 14 below).

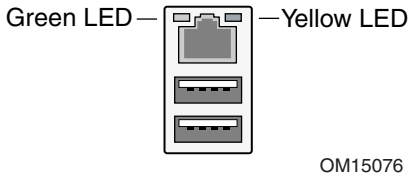


Figure 14. LAN Connector LED Locations

Table 7 describes the LED states when the board is powered up and the 10/100 Mbits/sec LAN subsystem is operating.

Table 7. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Mbits/sec data rate is selected.
	On	100 Mbits/sec data rate is selected.
Yellow	Off	LAN link is not established.
	On (steady state)	LAN link is established.
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN.

1.11.2 Gigabit LAN Subsystem

The Gigabit (10/100/1000 Mbits/sec) LAN subsystem includes the MCH (with its CSA interface), the Intel 82547EI PLC, and an RJ-45 LAN connector with integrated status LEDs.

1.11.2.1 Intel® 82547EI Platform LAN Connect Device

Intel 82547EI provides the following functions:

- Basic 10/100/1000 Ethernet LAN connectivity
- Communication Streaming Architecture (CSA) port provides higher throughput and lower latencies than the Intel 82562EZ device, resulting in up to 30% higher bus throughput (up to wirespeed)
- Full device driver compatibility
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

1.11.2.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (as shown in Figure 15). Table 8 describes the LED states when the board is powered up and the 10/100/1000 Mbits/sec LAN subsystem is operating.

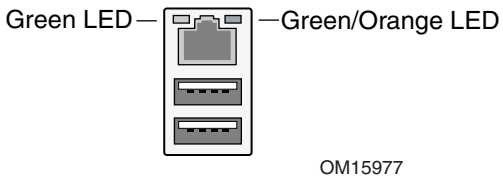


Figure 15. LAN Connector LED Locations

Table 8. LAN Connector LED States

LED	Color	LED State	Condition
Left	Green	Off	LAN link is not established.
		On (steady state)	LAN link is established.
		On (brighter and pulsing)	The computer is communicating with another computer on the LAN.
Right	Green	Off	10 Mbit/sec data rate is selected.
		On	100 Mbit/sec data rate is selected.
	Orange	On	1000 Mbit/sec data rate is selected.

1.11.3 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.2, page 16

1.12 Hardware Management Subsystem

The hardware management features enable the Desktop Board D865PERL to be compatible with the Wired for Management (WfM) specification. The Desktop Board D865PERL has the following hardware management features:

- Fan monitoring and control (through the I/O controller or the hardware monitoring and fan control ASIC)
- Thermal and voltage monitoring
- Chassis intrusion detection

For information about	Refer to
The WfM specification	Section 1.4, page 17

1.12.1.1 Hardware Monitoring and Fan Control ASIC

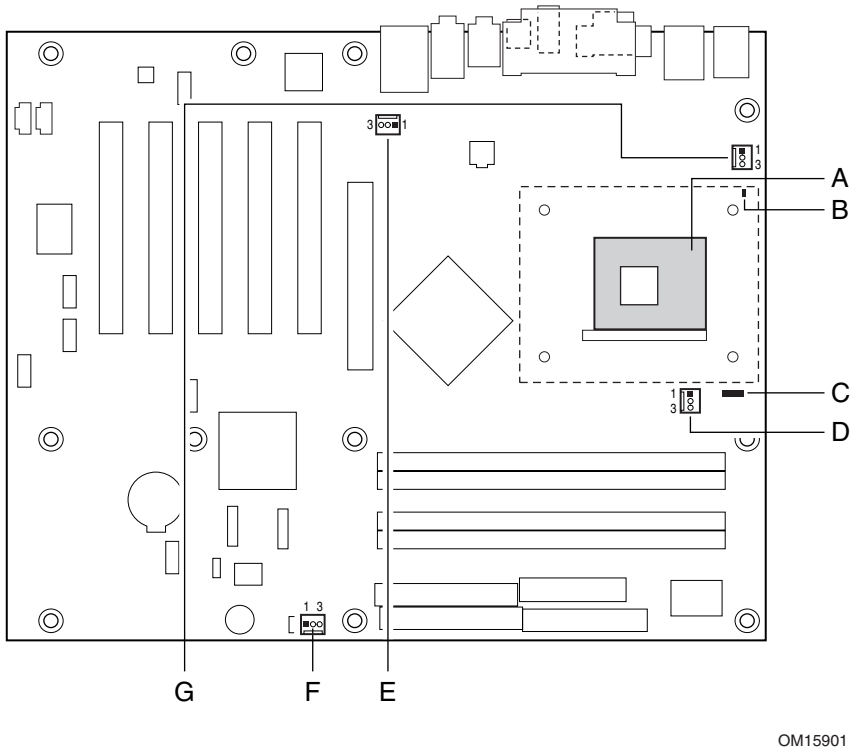
The features of the hardware monitoring and fan control ASIC (Standard Microsystems SMSC EMC6D101 or equivalent) include:

- Internal ambient temperature sensor
- Two remote thermal diode sensors for direct monitoring of processor temperature and ambient temperature sensing
- Power supply monitoring of five voltages (+5 V, +12 V, +3.3 V Standby, +1.5 V, and +VCCP) to detect levels above or below acceptable values
- Thermally monitored closed-loop fan control, for all three fans, that can adjust the fan speed or switch the fans on or off as needed
- SMBus interface

For information about	Refer to
The location of the fan connectors and sensors for thermal monitoring	Figure 16, page 42
The Standard Microsystems SMSC EMC6D101	http://www.smsc.com

1.12.1.2 Thermal Monitoring

Figure 16 shows the location of the sensors and fan connectors.



A Thermal diode, located on processor die
B Remote ambient temperature sensor
C Ambient temperature sensor (internal to hardware monitoring and fan control ASIC)
D Processor fan
E Rear chassis fan
F Front chassis fan
G Voltage regulator fan

Figure 16. Thermal Monitoring

1.12.2 Fan Monitoring

Fan monitoring can be implemented using Intel® Active Monitor, LANDesk* software, or third-party software.

For information about	Refer to
The functions of the fan connectors	Section 1.13.2.2, page 47

1.12.3 Chassis Intrusion and Detection

The boards support a chassis security feature that detects if the chassis cover has been removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion connector. When the chassis cover is removed, the mechanical switch is in the closed position.

For information about	Refer to
The location of the chassis intrusion connector	Figure 21, page 65
The signal names of the chassis intrusion connector	Table 35, page 67

1.13 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - LAN wake capabilities
  - Instantly Available PC technology
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 devices
  - Power Management Event (PME#) wake-up support

1.13.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the Desktop Board D865PERL requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the standby or sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 11 on page 46)
- Support for a front panel power and sleep mode switch

Table 9 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 9. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI S5 – Soft off)	Less than four seconds	Power-on (ACPI S0 – working state)
On (ACPI S0 – working state)	Less than four seconds	Soft-off/Standby (ACPI S1 or S3 – sleeping state)
On (ACPI S0 – working state)	More than four seconds	Fail safe power-off (ACPI S5 – Soft off)
Sleep (ACPI S1 or S3 – sleeping state)	Less than four seconds	Wake-up (ACPI S0 – working state)
Sleep (ACPI S1 or S3 – sleeping state)	More than four seconds	Power-off (ACPI S5 – Soft off)

For information about	Refer to
The Desktop Board D865PERL's compliance level with ACPI	Section 1.4, page 17

1.13.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 10 lists the power states supported by the Desktop Board D865PERL along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 10. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S1 – Processor stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 52.5 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/G5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.13.1.2 Wake-up Devices and Events

Table 11 lists the devices or specific events that can wake the computer from specific states.

Table 11. Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
LAN	S1, S3, S4, S5 (Note)
Modem (back panel Serial Port A)	S1, S3
PME#	S1, S3, S4, S5 (Note)
Power switch	S1, S3, S4, S5
PS/2 devices	S1, S3
RTC alarm	S1, S3, S4, S5
USB	S1, S3

Note: For LAN and PME#, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.13.2 Hardware Support

CAUTION

Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

The Desktop Board D865PERL provides power management hardware features, including:

- Power connector
- Fan connectors
- LAN wake capabilities
- Instantly Available PC technology
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# wake-up support

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal).

NOTE

The use of Resume on Ring and Wake from USB technologies from an ACPI state requires an operating system that provides full ACPI support.

1.13.2.1 Power Connector

ATX12V-compliant power supplies can turn off the system power through system control. When an ACPI-enabled system receives the correct command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The power connector locations	Figure 21, page 65
The power connector signal names	Table 33, page 67 and Table 30, page 66
The BIOS Setup program's Boot menu	Table 73, page 118
The ATX specification	Section 1.4, page 17

1.13.2.2 Fan Connectors

CAUTION

The processor fan must be connected to the processor fan connector, not to a chassis fan connector. Connecting the processor fan to a chassis fan connector may result in onboard component damage that will halt fan operation.

Table 12 summarizes the fan connector function/operation.

Table 12. Fan Connector Function/Operation

Connector	Description
Processor fan	• +12 V DC connection for a processor fan or active fan heatsink. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S3, S4, or S5 state. • Wired to a fan tachometer input of the hardware monitoring and fan control ASIC. • Closed-loop fan control that can adjust the fan speed or switch the fan on or off as needed. (Optional)
Front and rear chassis fans	• +12 V DC connection for a system or chassis fan. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S3, S4, or S5 state. • Wired to a fan tachometer input of the hardware monitoring and fan control ASIC. • Closed-loop fan control that can adjust the fan speed or switch the fan on or off as needed.
Voltage regulator fan	• +12 V DC connection for a system or chassis fan. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S3, S4, or S5 state. • Wired to a fan tachometer input of the hardware monitoring and fan control ASIC.

For information about:	Refer to:
The location of the fan connectors	Figure 21, page 65
The signal names of the fan connectors	Pages 66 and 67
The location of the fan connectors and sensors for thermal monitoring	Figure 16, page 42

1.13.2.3 LAN Wake Capabilities

⚠ CAUTION

For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the Desktop Board D865PERL supports LAN wake capabilities with ACPI in the following ways:

- PCI bus PME# signal for PCI 2.2 compliant LAN designs
- Onboard LAN subsystem

1.13.2.4 Instantly Available PC Technology

⚠ CAUTION

For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply.

Instantly Available PC technology enables the Desktop Board D865PERL to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 11 on page 46 lists the devices and events that can wake the computer from the S3 state.

The Desktop Board D865PERL supports the *PCI Bus Power Management Interface Specification*. For information on the version of this specification, see Section 1.4. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.2 compliant add-in cards and drivers.

1.13.2.5 Standby Power (+5 V) Indicator LED

CAUTION

If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the Desktop Board D865PERL. Failure to do so could damage the Desktop Board D865PERL and any attached devices.

The standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 17 shows the location of the standby power indicator LED.

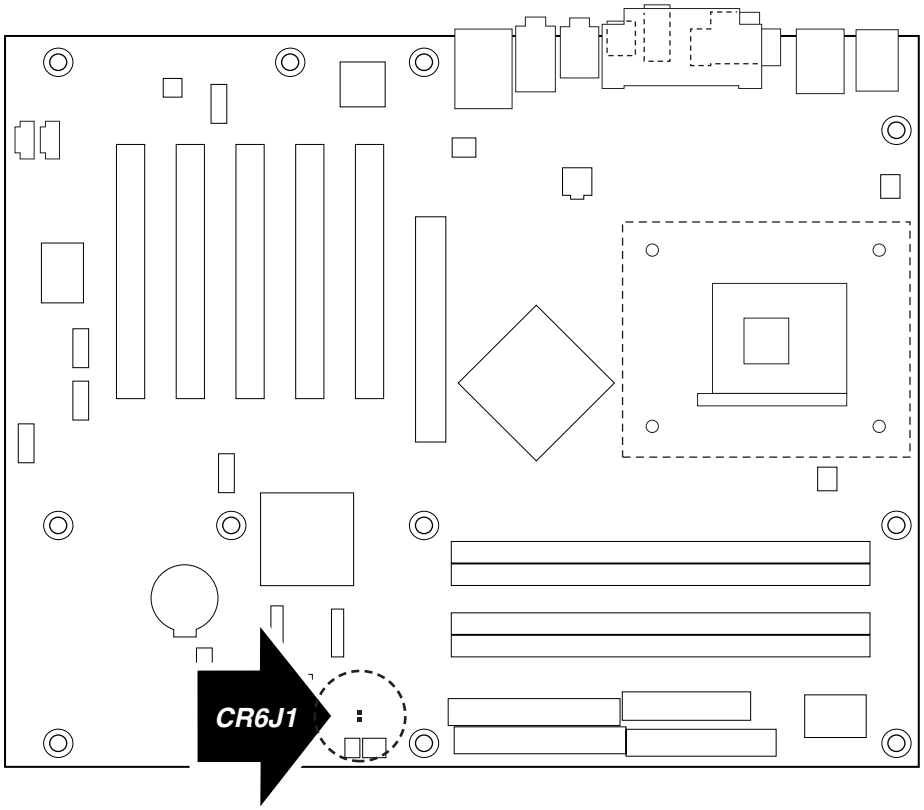


Figure 17. Location of the Standby Power Indicator LED

1.13.2.6 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from ACPI S1 or S3 states
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

1.13.2.7 Wake from USB

USB bus activity wakes the computer from an ACPI S1 or S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.13.2.8 Wake from PS/2 Devices

PS/2 device activity wakes the computer from an ACPI S1 or S3 state.

1.13.2.9 PME# Wake-up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state (with Wake on PME enabled in BIOS).

2 Technical Reference

What This Chapter Contains

2.1 Introduction

Sections 2.2 - 2.6 contain several standalone tables. Table 13 describes the system memory map, Table 14 lists the DMA channels, Table 15 shows the fixed I/O map, Table 16 defines the PCI configuration space map, and Table 17 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Resources

2.2.1 Addressable Memory

The D865PERL utilizes 4 GB of addressable system memory. Typically the address space that is allocated for PCI add-in cards, AGP aperture, BIOS (firmware hub), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 4 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- Memory-mapped I/O that is dynamically allocated for PCI and AGP cards
- AGP aperture
- APIC and chipset overhead (approximately 18 MB)
- BIOS/firmware hub (approximately 2 MB)

The amount of installed memory that can be used will vary based on add-in cards and BIOS settings. For example, if the PCI cards are requesting 200 MB of system memory and the AGP aperture is set to 256 MB in the BIOS Setup program, there will be approximately 3.54 GB of memory that can be accessed. Figure 18 shows a schematic of the system memory map. All installed system memory can be used when there is no overlap of system addresses. For example, all of the system address space can be utilized on a system that has 2 GB of installed system

memory, AGP aperture set for 256 MB, and the PCI cards are requesting 200 MB of system address space.

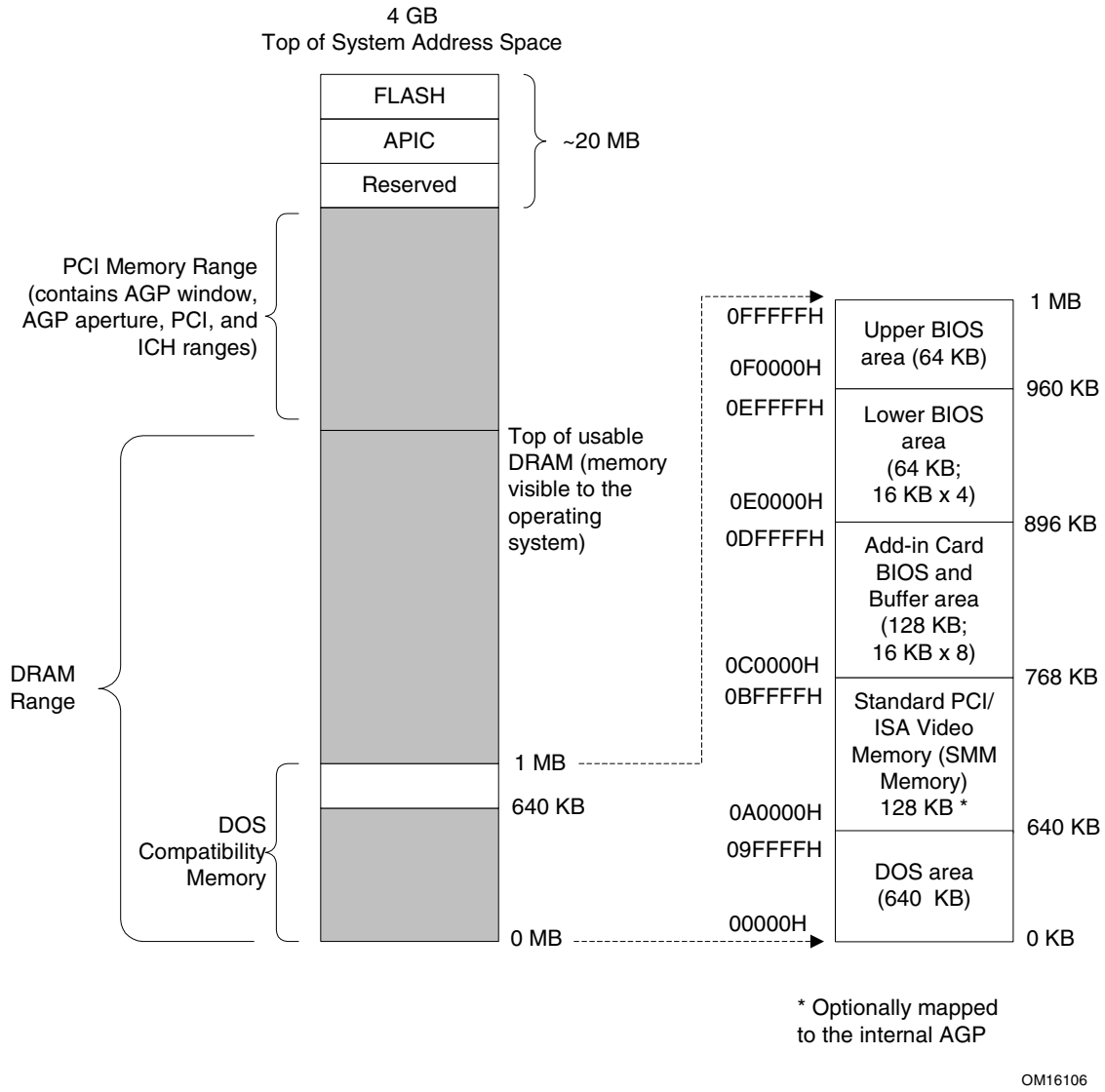


Figure 18. Detailed System Memory Address Map

2.2.2 Memory Map

Table 13 lists the system memory map.

Table 13. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 4194304 K	100000 - FFFFFFFF	4095 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Potential available high DOS memory (open to the PCI bus). Dependent on video adapter used.
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 DMA Channels

Table 14. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP or EPP)
4	8 or 16 bits	DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.4 Fixed I/O Map

Table 15. I/O Map

Address (hex)	Size	Description
0000 - 00FF	256 bytes	Used by the Desktop Board D865PERL. Refer to the ICH5 data sheet for dynamic addressing information
0170 - 0177	8 bytes	Secondary Parallel ATA IDE channel command block
01F0 - 01F7	8 bytes	Primary Parallel ATA IDE channel command block
0228 - 022F (Note 1)	8 bytes	LPT3
0278 - 027F (Note 1)	8 bytes	LPT2
02E8 - 02EF (Note 1)	8 bytes	COM4
02F8 - 02FF (Note 1)	8 bytes	COM2
0374 - 0377	4 bytes	Secondary Parallel ATA IDE channel control block
0378 - 037F	8 bytes	LPT1
03B0 - 03BB	12 bytes	Intel 82865PE MCH
03C0 - 03DF	32 bytes	Intel 82865PE MCH
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette channel
03F4 - 03F7	4 bytes	Primary Parallel ATA IDE channel control block
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 2)	4 bytes	PCI configuration address register
0CF9 (Note 3)	1 byte	Reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary Parallel ATA IDE bus master registers
FFA8 - FFAF	8 bytes	Secondary Parallel ATA IDE bus master registers

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

For information about	Refer to
ICH5 addressing	Section 1.2, page 16

2.5 PCI Configuration Space Map

Table 16. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82865PE component
00	01	00	Host to AGP bridge (virtual P2P)
00	03	00	PCI to CSA bridge (virtual P2P)
00	1E	00	Hub link to PCI bridge
00	1F	00	Intel 82801EB ICH5 PCI-to-LPC bridge
00	1F	01	Parallel ATA IDE controller
00	1F	02	Serial ATA controller
00	1F	03	SMBus controller
00	1F	05	AC ’97 audio controller
00	1F	06	AC ’97 modem controller (optional)
00	1D	00	USB UHCI controller 1
00	1D	01	USB UHCI controller 2
00	1D	02	USB UHCI controller 3
00	1D	03	USB UHCI controller 4
00	1D	07	EHCI controller
01	00	00	AGP add-in card
02	01	00	82547EI Gigabit LAN controller (optional)
(Note)	08	00	LAN controller
(Note)	00	00	PCI bus connector 1
(Note)	01	00	PCI bus connector 2
(Note)	02	00	PCI bus connector 3
(Note)	03	00	PCI bus connector 4
(Note)	04	00	PCI bus connector 5
(Note)	07	00	IEEE 1394a-2000 controller (optional)

Note: Bus number = 03 when the Intel 82547EI Gigabit LAN controller is used. Otherwise, bus number = 02.

2.6 Interrupts

The interrupts can be routed through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the ICH5 component. The PIC is supported in Windows 98 SE and Windows ME, and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP, and supports a total of 24 interrupts.

Table 17. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option)/User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	Reserved for ICH5 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE/Serial ATA (if present, else user available)
15	Secondary IDE/Serial ATA (if present, else user available)
16 (Note 2)	USB UHCI controller 1 and USB UHCI controller 4 (through PIRQA)
17 (Note 2)	AC ‘97 audio/modem/User available (through PIRQB)
18 (Note 2)	ICH5 USB controller 3 (through PIRQC)
19 (Note 2)	ICH5 USB controller 2 (through PIRQD)
20 (Note 2)	ICH5 LAN (through PIRQE)
21 (Note 2)	User available (through PIRQF)
22 (Note 2)	User available (through PIRQG)
23 (Note 2)	ICH5 USB 2.0 EHCI controller/User available (through PIRQH)

Notes:

1. Default, but can be changed to another IRQ.
2. Available in APIC mode only.

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH5 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the Desktop Board D865PERL and therefore share the same interrupt. Table 18 shows an example of how the PIRQ signals are routed.

For example, using Table 18 as a reference, assume an add-in card using INTA is plugged into PCI bus connector 3. In PCI bus connector 3, INTA is connected to PIRQB, which is already connected to the ICH5 audio controller. The add-in card in PCI bus connector 3 now shares an interrupt with the onboard interrupt source.

Table 18. PCI Interrupt Routing Map

PCI Interrupt Source	ICH5 PIRQ Signal Name							
	PIRQA	**PIRQB**	**PIRQC**	**PIRQD**	**PIRQE**	**PIRQF**	**PIRQG**	**PIRQH**
AGP connector	INTA	INTB						
ICH5 USB UHCI controller 1	INTA							
SMBus controller		INTB						
ICH5 USB UHCI controller 2				INTB				
AC '97 ICH5 Audio		INTB						
ICH5 LAN					INTA			
ICH5 USB UHCI controller 3			INTC					
ICH5 USB UHCI controller 4	INTA							
ICH5 USB 2.0 EHCI controller								INTD
PCI bus connector 1					INTD	INTA	INTB	INTC
PCI bus connector 2					INTC	INTB	INTA	INTD
PCI bus connector 3	INTD	INTA	INTB	INTC				
PCI bus connector 4			INTB	INTA		INTC	INTD	
PCI bus connector 5	INTC		INTA		INTD			INTB
Serial ATA/Serial ATA RAID						INTA		
IEEE-1394a-2000		INTA						

NOTE

In PIC mode, the ICH5 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. Refer to Table 17 for the allocation of PIRQ lines to IRQ signals in APIC mode.

2.8 Connectors

⚠ CAUTION

On the Desktop Board D865PERL, only the following connectors have overcurrent protection:

- *Back panel USB, IEEE 1394a-2000, and PS/2*
- *Front panel USB and IEEE 1394a-2000*

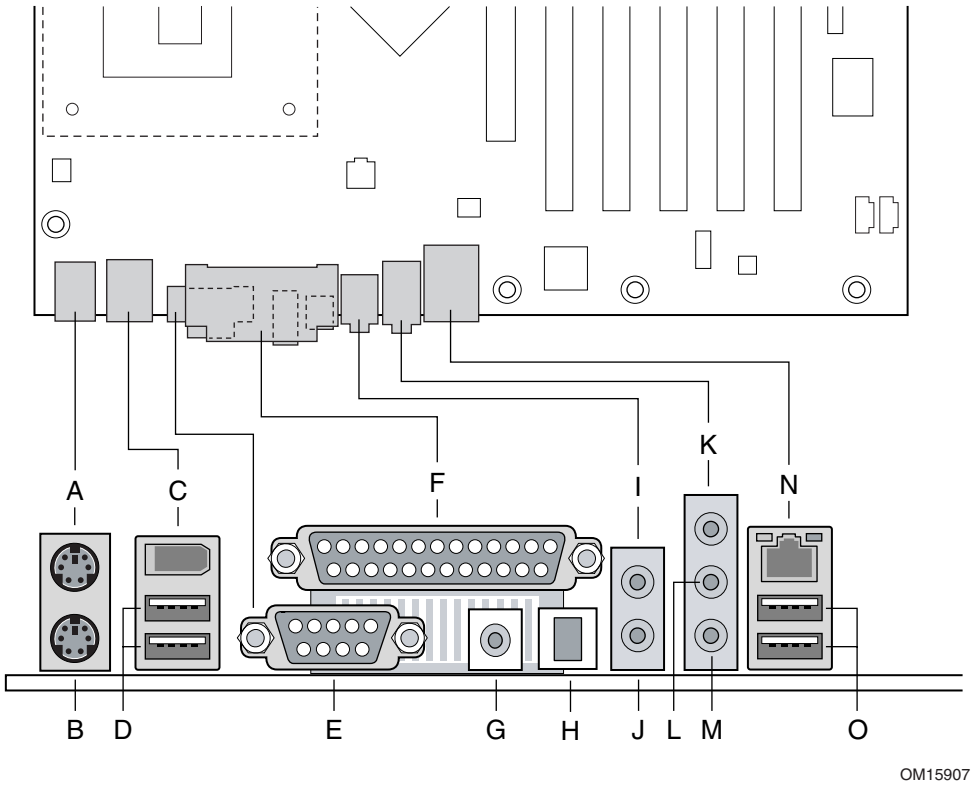
The other internal connectors of the Desktop Board D865PERL are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

The connectors are described on the following pages and are divided into these groups:

- Back panel I/O connectors (see page 60):
  - PS/2 keyboard and mouse
  - IEEE 1394a-2000 (optional)
  - USB
  - Parallel port
  - Serial port A
  - Coaxial S/PDIF (optional)
  - Optical S/PDIF (optional)
  - Audio
  - LAN
- Internal I/O connectors (see page 61):
  - ATAPI-style auxiliary line input
  - ATAPI CD-ROM
  - Front panel audio
  - Fans [four]
  - Power
  - PCI add-in boards
  - AGP add-in board
  - Parallel ATA IDE
  - Diskette drive
  - Serial ATA
- External I/O connectors (see page 70):
  - Auxiliary front panel power, sleep, and message-waiting LED
  - Front panel (power, sleep, and message-waiting LED; power switch; hard drive activity LED; and reset switch)
  - Front panel USB [two]
  - Front panel IEEE 1394a-2000 (optional) [two]

2.8.1 Back Panel Connectors

Figure 19 shows the location of the back panel connectors. The back panel connectors are color-coded in compliance with PC 99 recommendations. The figure legend below lists the colors used.



Item	Description	Color
A	PS/2 mouse port	Green
B	PS/2 keyboard port	Purple
C	IEEE 1394a-2000 port (optional)	Black
D	USB ports [two]	Black
E	Serial port A	Teal
F	Parallel port	Burgundy
G	Coaxial S/PDIF (optional)	Orange
H	Optical S/PDIF (optional)	Black/Gray
I	Audio rear left and right out (for 6-channel audio only)	Black
J	Audio center and LFE out (for 6-channel audio only)	Black
K	Audio line in	Light blue
L	Audio front left and right out	Lime green
M	Mic in	Pink
N	LAN	Black
O	USB ports [two]	Black

Figure 19. Back Panel Connectors

NOTE

Powered speakers are required.

Table 19. Coaxial S/PDIF Connector (Optional)

Pin	Signal Name
Tip	S/PDIF
Sleeve	Ground

Table 20. Optical S/PDIF Connector (Optional)

Location	Signal Name
Tunnel	S/PDIF

Table 21. Audio Rear Left and Right Out Connector (Optional)

Pin	Signal Name
Tip	Rear left out
Ring	Rear right out
Sleeve	Ground

Table 22. Audio Center and LFE Out Connector (Optional)

Pin	Signal Name
Tip	Center out
Ring	LFE out
Sleeve	Ground

Table 23. Audio Line In Connector

Pin	Signal Name
Tip	Audio left in
Ring	Audio right in
Sleeve	Ground

Table 24. Audio Line Out Connector (Front Left and Right Out for 6-Channel Audio)

Pin	Signal Name
Tip	Audio left out
Ring	Audio right out
Sleeve	Ground

Table 25. Mic In Connector

Pin	Signal Name
Tip	Mono in
Ring	Mic bias voltage
Sleeve	Ground

2.8.2 Internal I/O Connectors

The internal I/O connectors are divided into the following functional groups:

- Audio (see page 63):
  - ATAPI-style auxiliary line input
  - ATAPI CD-ROM
  - Front panel audio
- Power and hardware control (see page 65):
  - Fans [four]
  - ATX12V
  - Main power
  - Chassis intrusion
- Add-in boards and peripheral interfaces (see page 68):
  - PCI bus
  - AGP
  - Parallel ATA IDE [two]
  - Serial ATA [two]
  - Diskette drive

2.8.2.1 Expansion Slots

The Desktop Board D865PERL has the following expansion slots:

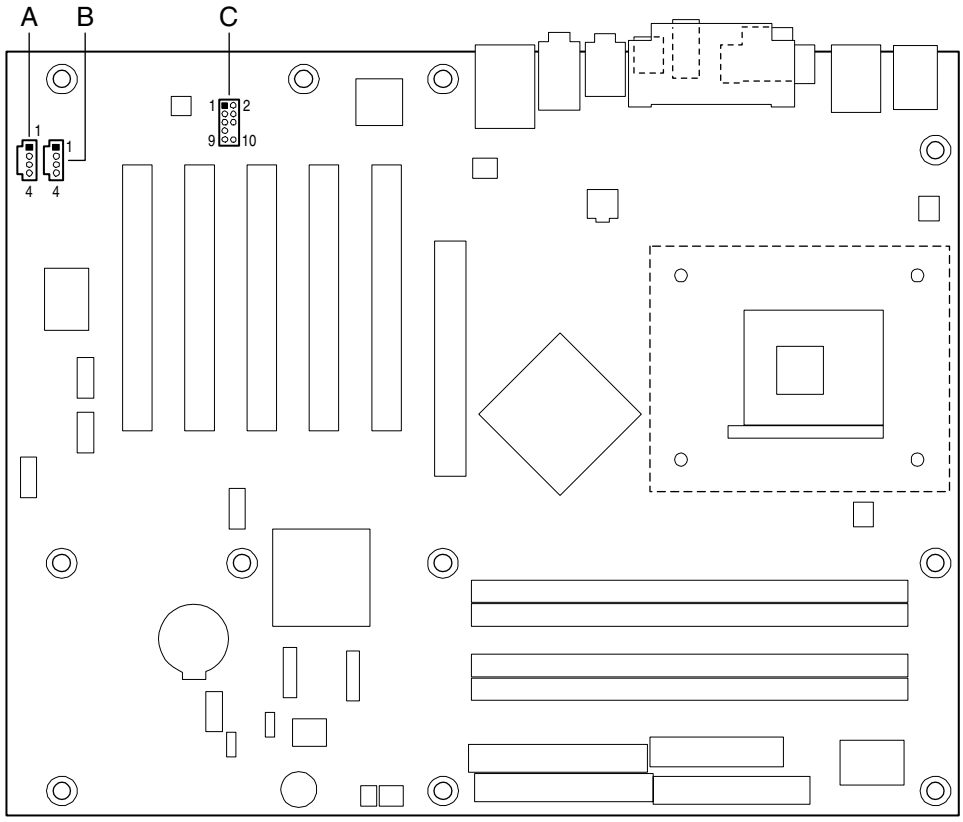
- AGP connector: The AGP connector is keyed for Universal 0.8 V AGP 3.0 cards or 1.5 V AGP 2.0 cards only. Do not install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.
- Five PCI rev 2.2 compliant local bus slots: PCI add-in cards with SMBus support can access sensor data and other information residing on the Desktop Board D865PERL.

NOTE

This document references back-panel slot numbering with respect to processor location on the board. The AGP slot is not numbered. PCI slots are identified as PCI slot #x, starting with the slot closest to the processor. Figure 22 on page 68 illustrates the board's PCI slot numbering.

2.8.2.2 Audio Connectors

Figure 21 shows the location of the audio connectors.



Item	Description	For more information see:
A	ATAPI-style auxiliary line input	Table 26
B	ATAPI CD-ROM	Table 27
C	Front panel audio	Table 28

Figure 20. Audio Connectors

Table 26. Auxiliary Line Input Connector

Pin	Signal Name
1	Left auxiliary line in
2	Ground
3	Ground
4	Right auxiliary line in

Table 27. ATAPI CD-ROM Connector

Pin	Signal Name
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

Table 28. Front Panel Audio Connector

Pin	Signal Name	Pin	Signal Name
1	Mono Mic in (Stereo Mic 1)	2	Ground
3	Mono Mic Bias (Stereo Mic 2)	4	+5 V
5	RIGHT_OUT	6	Right channel return
7	Not connected	8	Key
9	LEFT_OUT	10	Left channel return

NOTE

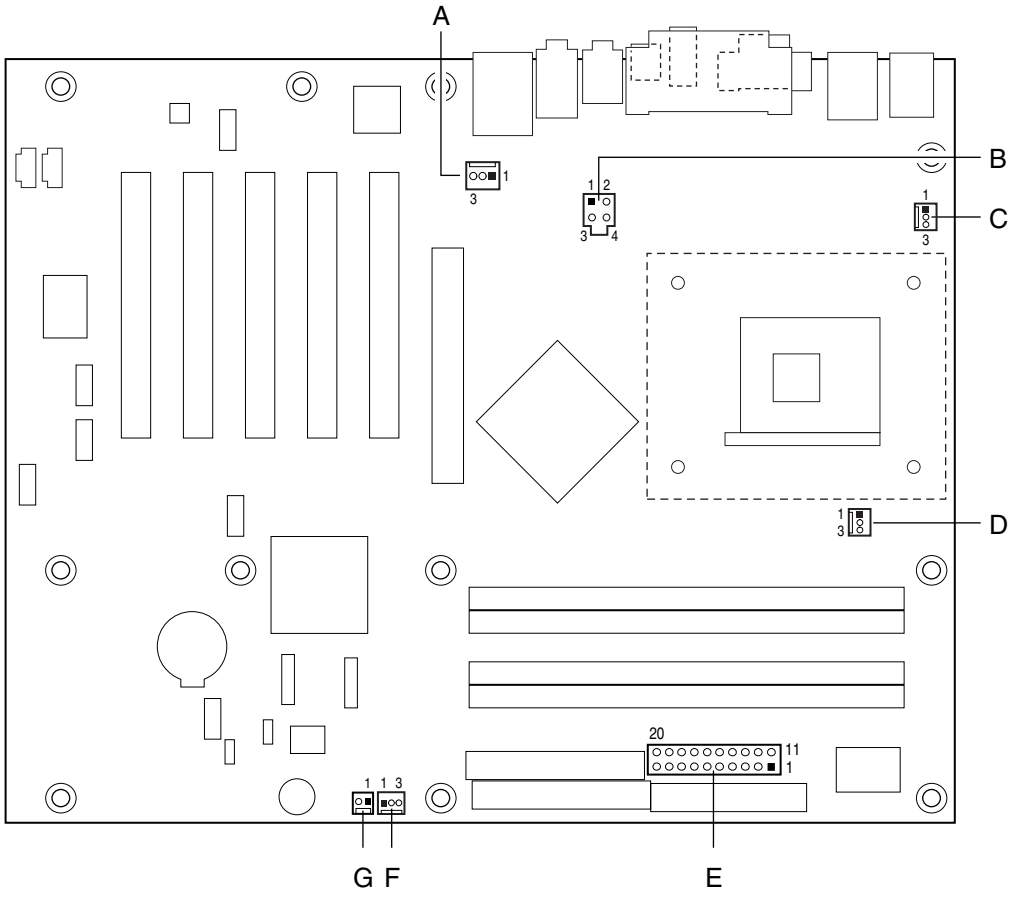
The front panel audio connector is alternately used as a jumper block for routing audio signals. For more information, see Section 2.9.1 on page 74.

2.8.2.3 Power and Hardware Control Connectors

CAUTION

The processor fan must be connected to the processor fan connector, not to a chassis fan connector. Connecting the processor fan to a chassis fan connector may result in onboard component damage that will halt fan operation.

Figure 21 shows the location of the power and hardware control connectors.



Item	Description	For more information see:
A	Rear chassis fan	Table 29
B	+12 V power connector (ATX12V)	Table 30
C	Voltage regulator fan	Table 31
D	Processor fan	Table 32
E	Main power	Table 33
F	Front chassis fan	Table 34
G	Chassis intrusion	Table 35

Figure 21. Power and Hardware Control Connectors

NOTE

Do not use a standard ATX power supply. The Desktop Board D865PERL will not boot with a standard ATX power supply. Use only ATX12V-compliant power supplies with the Desktop Board D865PERL. ATX12V power supplies have an additional power lead that provides required supplemental power for the Intel Pentium 4 processor. The Desktop Board D865PERL will not boot if the ATX12V power supply is not connected to both the 4-pin and 20-pin power connectors.

For information about	Refer to
The power connector	Section 1.13.2.1, page 47
The functions of the fan connectors	Section 1.13.2.2, page 47

Table 29. Rear Chassis Fan Connector

Pin	Signal Name
1	Control
2	+12 V
3	TACH

Table 30. ATX12V Power Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Ground
3	+12 V	4	+12 V

Table 31. Voltage Regulator Fan Connector

Pin	Signal Name
1	Ground / Control
2	+12 V
3	TACH

Table 32. Processor Fan Connector

Pin	Signal Name
1	Ground / Control
2	+12 V
3	TACH

Table 33. Main Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	Not connected
9	+5 V (Standby)	19	+5 V
10	+12 V	20	+5 V

Table 34. Front Chassis Fan Connector

Pin	Signal Name
1	Control
2	+12 V
3	TACH

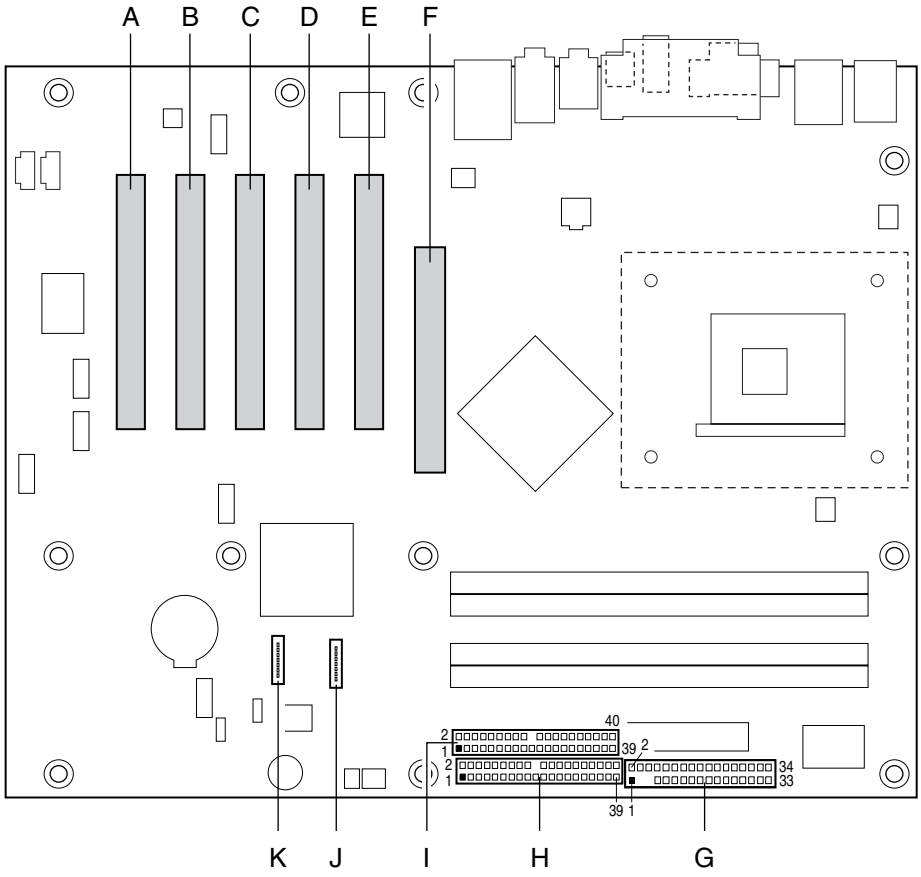
Table 35. Chassis Intrusion Connector

Pin	Signal Name
1	Intruder
2	Ground

2.8.2.4 Add-in Board and Peripheral Interface Connectors

Figure 22 shows the location of the add-in board and peripheral connectors for the Desktop Board D865PERL. Note the following considerations for the PCI bus connectors:

- All of the PCI bus connectors are bus master capable.
- The SMBus is routed to PCI bus connector 2. This enables PCI bus add-in boards with SMBus support to access sensor data on the Desktop Board D865PERL. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40
  - The SMBus data line is connected to pin A41



OM15909

Item	Description	Item	Description
A	PCI bus connector 5	G	Diskette drive
B	PCI bus connector 4	H	Primary Parallel ATA IDE [black]
C	PCI bus connector 3	I	Secondary Parallel ATA IDE [white]
D	PCI bus connector 2	J	Serial ATA connector 1
E	PCI bus connector 1	K	Serial ATA connector 0
F	AGP		

Figure 22. D865PERL Add-in Board and Peripheral Interface Connectors

NOTE

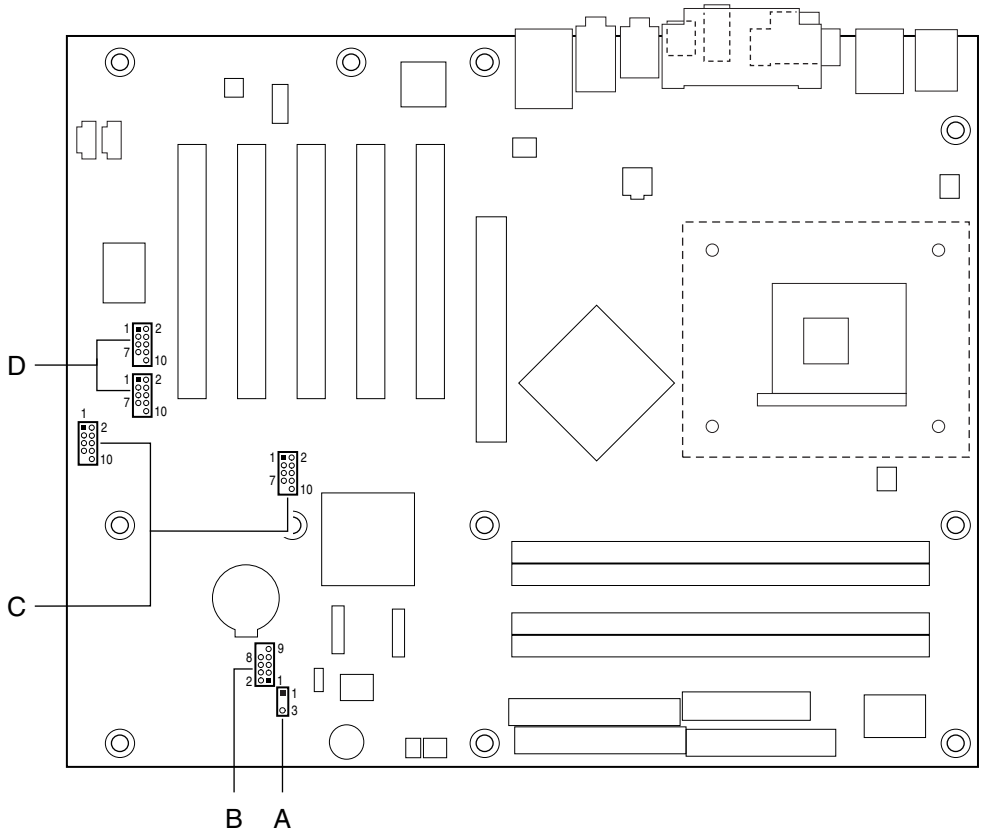
The AGP connector is keyed for universal 0.8 V AGP 3.0 cards or 1.5 V AGP 2.0 cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards

Table 36. Serial ATA Connectors

Pin	Signal Name
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7	Ground

2.8.3 External I/O Connectors

Figure 23 shows the locations of the external I/O connectors.



Item	Description	Color	For more information see:
A	Auxiliary front panel power/sleep/ message-waiting LED	Black	Table 37
B	Front panel	White	Table 38
C	Front panel USB (2)	Black	Figure 25
D	Front panel IEEE 1394a-2000 (2) (optional)	Blue	Figure 26

Figure 23. External I/O Connectors

2.8.3.1 Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector

Pins 1 and 3 of this connector duplicate the signals on pins 2 and 4 of the front panel connector.

Table 37. Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	Not connected		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.8.3.2 Front Panel Connector

This section describes the functions of the front panel connector. Table 38 lists the signal names of the front panel connector. Figure 24 is a connection diagram for the front panel connector.

Table 38. Front Panel Connector

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
Hard Drive Activity LED				**Power LED**			
1	HD_PWR	Out	Hard disk LED pull-up (750 Ω) to +5 V	2	HDR_BLNK_ GRN	Out	Front panel green LED
3	HAD#	Out	Hard disk active LED	4	HDR_BLNK_ YEL	Out	Front panel yellow LED
Reset Switch				**On/Off Switch**			
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
Power				**Not Connected**			
9	+5 V		Power	10	N/C		Not connected–

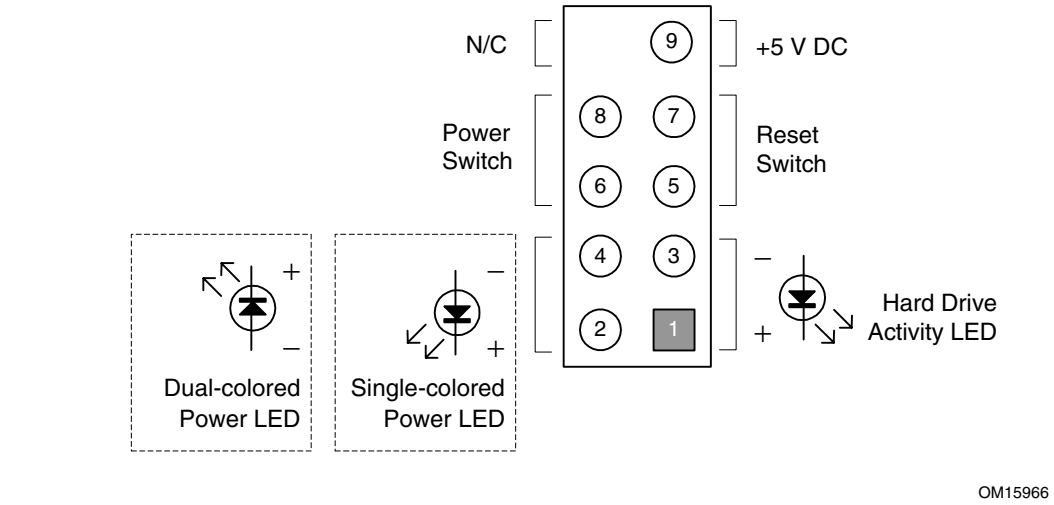


Figure 24. Connection Diagram for Front Panel Connector

2.8.3.2.1 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires one of the following:

- A Serial ATA hard drive connected to an onboard Serial ATA connector
- A Parallel ATA IDE hard drive connected to an onboard Parallel ATA IDE connector

2.8.3.2.2 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the Desktop Board D865PERL resets and runs the POST.

2.8.3.2.3 Power/Sleep/Message Waiting LED Connector

Pins 2 and 4 can be connected to a one- or two-color LED. Table 39 shows the possible states for a one-color LED. Table 40 shows the possible states for a two-color LED.

Table 39. States for a One-Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running
Blinking Green	Running/message waiting

Table 40. States for a Two-Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

NOTE

To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

2.8.3.2.4 Power Switch Connector

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the Desktop Board D865PERL.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.8.3.3 Front Panel USB Connectors

Figure 25 is a connection diagram for the front panel USB connectors.

INTEGRATOR'S NOTES

- *The +5 V DC power on the USB connector is fused.*
- *Pins 1, 3, 5, and 7 comprise one USB port.*
- *Pins 2, 4, 6, and 8 comprise one USB port.*
- *Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.*

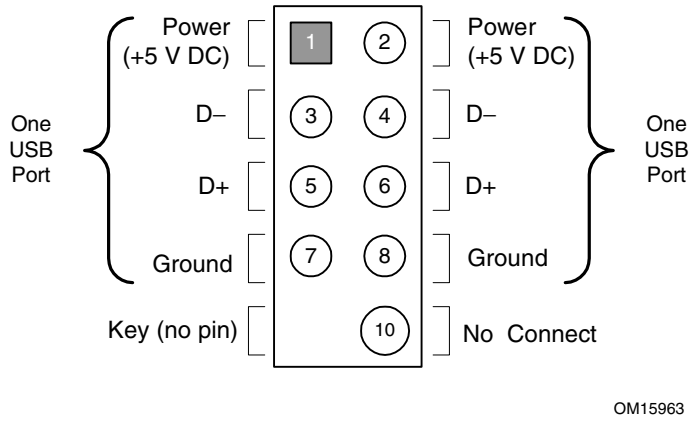


Figure 25. Connection Diagram for Front Panel USB Connectors

2.8.3.4 Front Panel IEEE 1394a-2000 Connectors (Optional)

Figure 26 is a connection diagram for the front panel IEEE 1394a-2000 connectors.

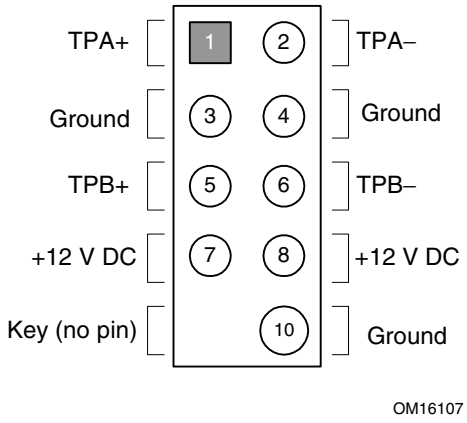


Figure 26. Connection Diagram for Front Panel IEEE 1394a-2000 Connectors

INTEGRATOR'S NOTES

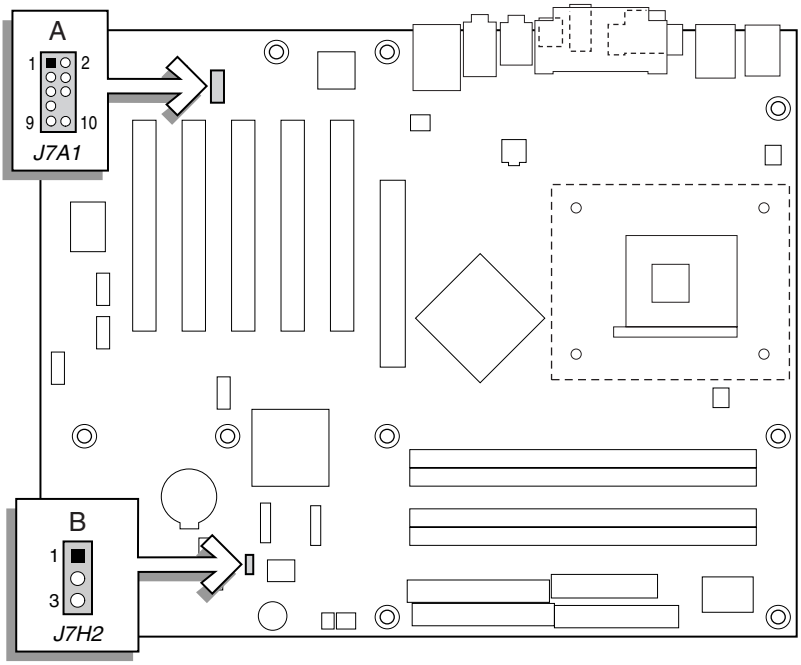
- *The +12 V DC power on the IEEE 1394a-2000 connectors is fused.*
- *Each IEEE 1394a-2000 connector provides one IEEE 1394a-2000 port.*

2.9 Jumper Blocks

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the Desktop Board D865PERL could be damaged.

Figure 27 shows the location of the jumper blocks on the Desktop Board D865PERL.



Item	Description	Reference Designator
A	Front panel audio connector/jumper block	J7A1
B	BIOS Setup configuration jumper block	J7H2

Figure 27. Location of the Jumper Blocks

2.9.1 Front Panel Audio Connector/Jumper Block

CAUTION

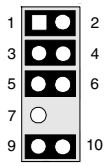
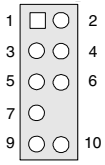
Do not place jumpers on this block in any configuration other than the one described in Table 41. Other jumper configurations are not supported and could damage the Desktop Board D865PERL.

This connector has two functions:

- With jumpers installed, the audio line out signals are routed to the back panel audio line out connector.
- With jumpers removed, the connector provides audio line out and mic in signals for front panel audio connectors.

Table 41 describes the two configurations of this connector/jumper block.

Table 41. Front Panel Audio Connector or Jumper Block

Jumper Setting		Configuration
	1 and 2 3 and 4 5 and 6 9 and 10	Front out signals if 6-channel audio (line out signals if 2-channel audio) are routed to the back panel line out connector. The back panel audio line out connector is shown in Figure 19 on page 60.
	No jumpers installed	Mic in and front out signals if 6-channel audio (line out signals if 2-channel audio) are available for connection to front panel audio connectors. Table 28 on page 64 lists the names of the signals available on this connector when no jumpers are installed.

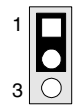
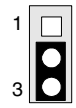
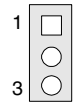
NOTE

When the jumpers are removed and this connector is used for front panel audio, the back panel audio line out and mic in connectors are disabled.

2.9.2 BIOS Setup Configuration Jumper Block

The 3-pin jumper block determines the BIOS Setup program's mode. Table 42 describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configure mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

Table 42. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

For information about	Refer to
How to access the BIOS Setup program	Section 4.1, page 95
The maintenance menu of the BIOS Setup program	Section 4, page 95
BIOS recovery	Section 0, page 91

2.10 Mechanical Considerations

2.10.1 D865PERL Form Factor

The Desktop Board D865PERL is designed to fit into an ATX-form-factor chassis. In Figure 28, dimensions are given in inches [millimeters]. The outer dimensions of the board are 12.0 inches by 9.6 inches [304.80 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification (see Section 1.4).

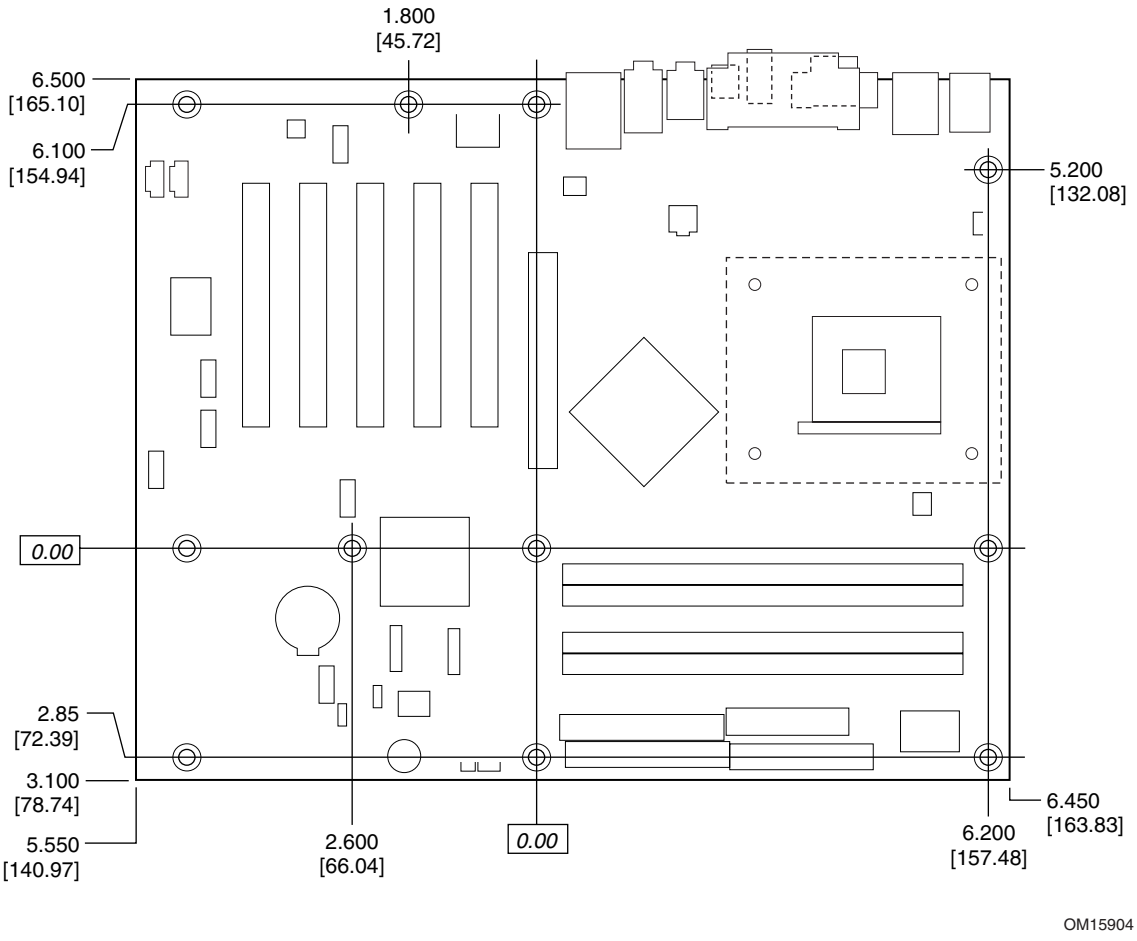


Figure 28. Board Dimensions

2.10.2 I/O Shield

The back panel I/O shield for Desktop Board D865PERL must meet specific dimension and material requirements. Systems based on the Desktop Board D865PERL need the back panel I/O shield to pass certification testing. Figure 29 show the critical dimensions of the I/O shield for the Desktop Board D865PERL.

The figure indicates the position of each cutout and gives dimensions in inches to a tolerance of ±0.02 inches. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 1.4 for information about the ATX specification.

NOTE

The I/O shield drawings in this document are for reference only. An I/O shield compliant with the ATX chassis specification 2.03 is available from Intel.

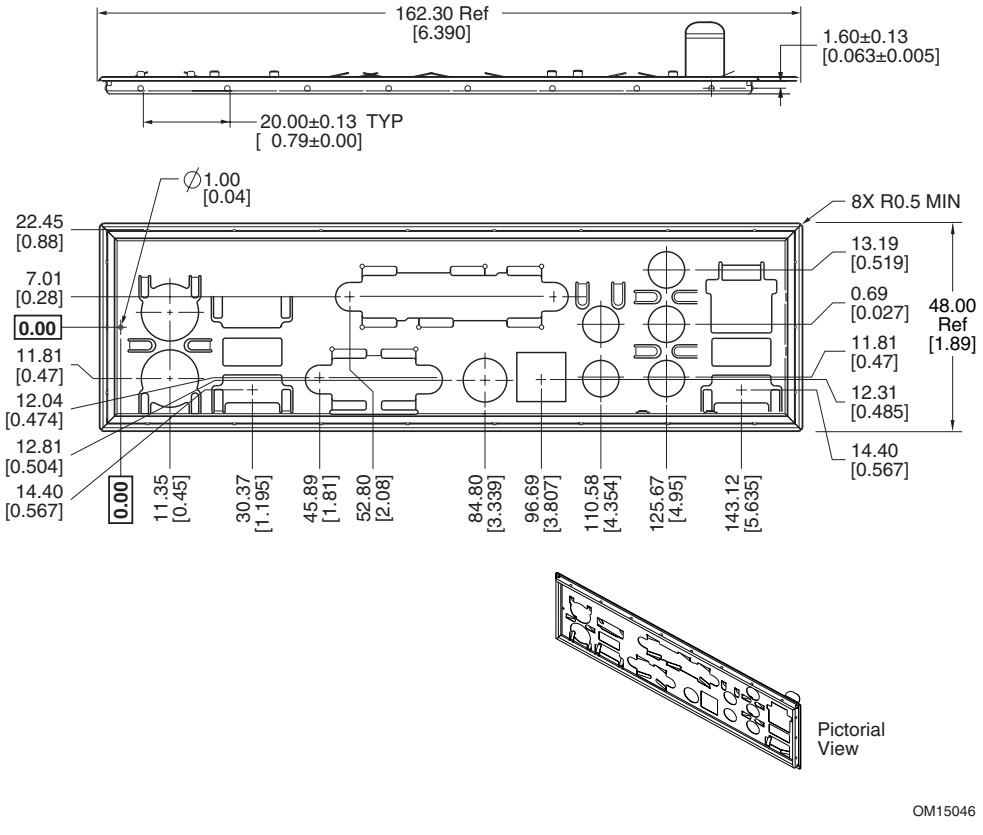


Figure 29. I/O Shield Dimensions

2.11 Electrical Considerations

2.11.1 DC Loading

Table 43 lists the DC loading characteristics of the board.

Table 43. DC Loading Characteristics

Mode	DC Power	DC Current at:				
		+3.3 V	+5 V	+12 V	-12 V	+5 VSB
Minimum loading	196 W	6 A	11 A	9 A	0.03 A	0.80 A
Maximum loading	330 W	12 A	15 A	16 A	0.10 A	1.60 A

2.11.2 Add-in Board Considerations

The Desktop Board D865PERL is designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards for a fully loaded Desktop Board D865PERL (all five expansion slots and the AGP slot filled) must not exceed 12 A.

2.11.3 Fan Connector Current Capability

⚠ CAUTION

The processor fan must be connected to the processor fan connector, not to a chassis fan connector. Connecting the processor fan to a chassis fan connector may result in onboard component damage that will halt fan operation.

Table 44 lists the current capability of the fan connectors on the Desktop Board D865PERL.

Table 44. Fan Connector Current Capability

Fan Connector	Maximum Available Current
Processor fan	1600 mA
Front chassis fan	600 mA
Rear chassis fan	600 mA
Voltage regulator fan	1000 mA

2.11.4 Power Supply Considerations

⚠ CAUTION

The +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

System integrators should refer to the power usage values listed in Table 43 when selecting a power supply for use with the Desktop Board D865PERL.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

For information about	Refer to
The ATX form factor specification	Section 1.4, page 17

2.12 Thermal Considerations

CAUTION

The use of an Intel Pentium 4 processor operating above 2.80 GHz with this Intel desktop board requires the following:

- *A chassis with appropriate airflow to ensure proper cooling of the components on the board*
- *A processor fan heatsink that meets the thermal performance targets for Pentium 4 processors operating above 2.80 GHz*

Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the desktop board. For a list of chassis that have been tested with Intel desktop boards please refer to the following website:

http://developer.intel.com/design/motherbd/cooling.htm

All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.

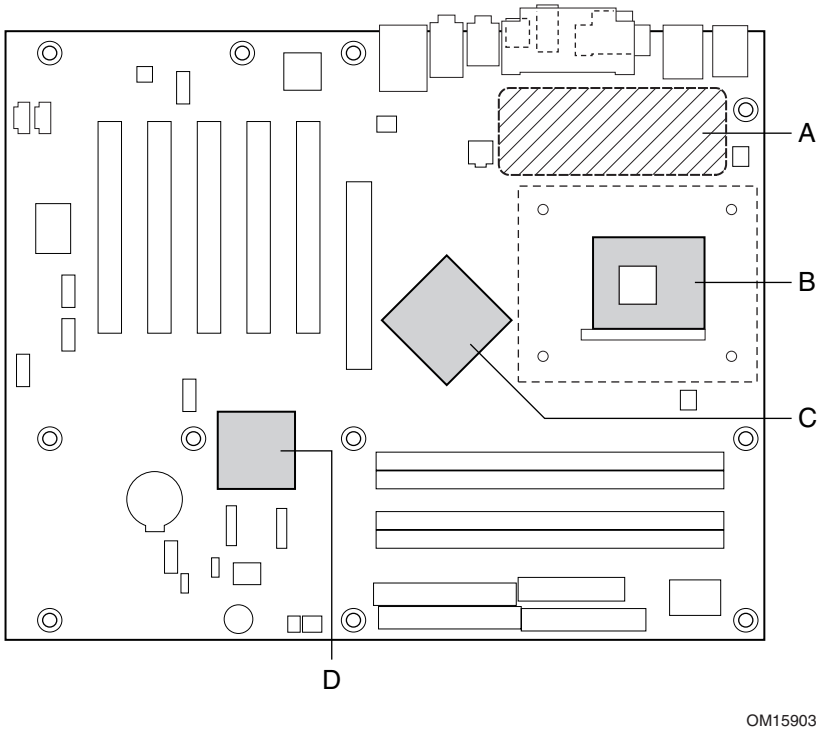
CAUTION

Ensure that the ambient temperature does not exceed the Desktop Board D865PERL's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (item A in Figure 30) can reach a temperature of up to 85 °C in an open chassis.

Figure 30 shows the locations of the localized high temperature zones.



Item	Description
A	Processor voltage regulator area
B	Processor
C	Intel 82865PE MCH
D	Intel 82801EB ICH5 or 82801ER ICH5-R

Figure 30. Localized High Temperature Zones

Table 45 provides maximum case temperatures for components on the Desktop Board D865PERL that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the Desktop Board D865PERL.

Table 45. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium 4 processor	For processor case temperature, see processor datasheets and processor specification updates
Intel 82865PE MCH	99 °C (under bias)
Intel 82801EB ICH5 or 82801ER ICH5-R	115 °C (under bias)

For information about	Refer to
Intel Pentium 4 processor datasheets and specification updates	Section 1.2, page 16

2.13 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data is calculated from predicted data at 55 ºC. The MTBF calculation for the Desktop Board D865PERL is 101,376 hours.

2.14 Environmental

Table 46 lists the environmental specifications for the Desktop Board D865PERL.

Table 46. Desktop Board D865PERL Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the Desktop Boards' compliance with U.S. and international safety and electromagnetic compatibility (EMC) regulations.

2.15.1 Safety Regulations

Table 47 lists the safety regulations the Desktop Board D865PERL complies with when correctly installed in a compatible host system.

Table 47. Safety Regulations

Regulation	Title
UL 60950 3rd ed.,2000/CSA C22.2 No. 60950-00	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950:2000	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC 60950, 3rd Edition, 1999	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

2.15.2 EMC Regulations

Table 48 lists the EMC regulations the Desktop Board D865PERL complies with when correctly installed in a compatible host system.

Table 48. EMC Regulations

Regulation	Title
FCC (Class B)	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radio Frequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022: 1998 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS 3548 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 3rd Edition (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurements. (International)

2.15.2.1 FCC Compliance Statement (USA)

Product Type: D865PERL Desktop Board

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to a different electrical branch circuit from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications to the equipment not expressly approved by Intel Corporation could void the user's authority to operate the equipment.

2.15.2.2 Canadian Compliance Statement

This Class B digital apparatus complies with Canadian ICES-003.

Cet appereil numérique de la classe B est conforme à la norme NMB-003 du Canada.

2.15.3 European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the product: Intel® Desktop Board D865PERL is in conformity with all applicable essential requirements necessary for CE marking, following the provisions of the European Council Directive 89/336/EEC (EMC Directive) and Council Directive 73/23/EEC (Safety/Low Voltage Directive).

The product is properly CE marked demonstrating this conformity and is for distribution within all member states of the EU with no restrictions.

This product follows the provisions of the European Directives 89/336/EEC and 73/23/EEC.

2.15.4 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

2.15.4.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

2.15.4.2 Recycling Considerations

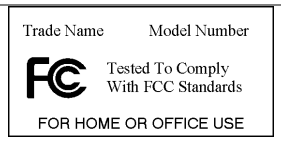
Intel encourages its customers to recycle its products and their components (e.g., batteries, circuit boards, plastic enclosures, etc.) whenever possible. In the U.S., a list of recyclers in your area can be found at:
http://www.eiae.org

In the absence of a viable recycling option, products and their components must be disposed of in accordance with all applicable local environmental regulations.

2.15.5 Product Certification Markings (Board Level)

Table 49 lists the board's product certification markings.

Table 49. Product Certification Markings

Description	Marking
UL joint US/Canada Recognized Component mark. Includes adjacent UL file number for Intel Desktop Boards: E210882 (component side).	
FCC Declaration of Conformity logo mark for Class B equipment; includes Intel name and D865PERL model designation (component side).	
CE mark. Declares compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC) (component side). The CE mark should also be on the shipping container.	
Australian Communications Authority (ACA) C-Tick mark. Includes adjacent Intel supplier code number, N-232. The C-tick mark should also be on the shipping container.	
Printed wiring board manufacturer's recognition mark: consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side).	94V-0

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The Desktop Board uses an Intel/AMI BIOS that is stored in the Firmware Hub (FWH) and can be updated using a disk-based program. The FWH contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as RL86510A.86A.

When the BIOS Setup configuration jumper is set to configure mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

For information about	Refer to
The Desktop Board's compliance level with Plug and Play	Section 1.4, page 17

3.2 BIOS Flash Memory Organization

The Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

For information about	Refer to
The versions of PCI and Plug and Play supported by the BIOS	Section 1.4, page 17

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.4 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags

- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and logging

Non-Plug and Play operating systems require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The compliance level of the Desktop Board D865PERL with SMBIOS	Section 1.4, page 17

3.5 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities support the following BIOS maintenance functions:

- Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.
- Updating both the BIOS boot block and the main BIOS. This process is fault tolerant to prevent boot block corruption.
- Updating the BIOS boot block separately.
- Changing the language section of the BIOS.
- Updating replaceable BIOS modules, such as the video BIOS module.
- Inserting a custom splash screen.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 16

3.6.1 Language Support

The BIOS Setup program and help messages are supported in six languages: US English, German, Italian, French, Spanish, and Japanese. Only two languages (US English and another language) can be loaded on the board at one time.

The default language for the BIOS Setup program and help messages is US English. Another language can be selected by using the program's Main menu (page 97).

3.6.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be augmented with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site.

NOTE

If you add a custom splash screen, it will share space with the Intel branded logo.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 16

3.7 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a 1.44 MB diskette or CD-ROM using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is no video support. You can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Update Utility are available from Intel Customer Support through the Intel World Wide Web site.

✏ NOTE

Even if the computer is configured to boot from an LS-120 diskette (in the Setup program's Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
The BIOS recovery mode jumper settings	Section 2.9.1, page 74
The Boot menu in the BIOS Setup program	Section 4.3, page 97
Contacting Intel customer support	Section 1.2, page 16

3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

3.8.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

For information about	Refer to
The El Torito specification	Section 1.4, page 17

3.8.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or from a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

For information about	Refer to
The BIOS Setup program's Security menu	Table 70, page 116

3.8.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.8.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

For information about	Refer to
The BIOS Setup program's Security menu	Table 70, page 116

The menu displayed after pressing the <F10> key lists the available boot devices (as set in the BIOS Setup program's Boot Device Priority submenu). Table 50 lists the boot device menu options.

Table 50. Boot Device Menu Options

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, saves changes, and boots from the selected device
<Esc>	Exits the menu without making changes

3.9 Fast Booting Systems with Intel® Rapid BIOS Boot

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel® Rapid BIOS

3.9.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as "power-up to data ready" less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

3.9.2 Intel Rapid BIOS Boot

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot menu:

- Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- Disable Quiet Boot, which eliminates display of the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Enable Intel Rapid BIOS Boot. This feature bypasses memory count and the search for a diskette drive.

In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

✎ NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from three to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced menu in the Drive Configuration Submenu of the BIOS Setup program).

For information about	Refer to
Drive Configuration Submenu in the BIOS Setup program	Section 4.4.4, page 103

3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives access to view and change Setup options in the BIOS Setup program based on the setting of the User Access Level option in the BIOS Setup program's Security menu. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the BIOS Setup program's password prompt allows the user access to Setup based on the setting of the User Access Level option in the BIOS Setup program's Security menu.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 51 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 51. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

For information about	Refer to
Setting user and supervisor passwords	Section 4.4.11, page 115

✏ NOTES

- *For enhanced security, use different passwords for the supervisor and user passwords.*
- *Valid password characters are A-Z, a-z, and 0-9.*

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

Table 52 lists the BIOS Setup program menu features.

Table 52. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and displays processor information	Displays processor and memory configuration	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features and power supply controls	Selects boot options	Saves or discards changes to Setup program options

NOTE

In this chapter, all examples of the BIOS Setup program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the Desktop Board is in configure mode. Section 2.9.2 on page 75 tells how to put the Desktop Board in configure mode.

Table 53 lists the function keys available for menu screens.

Table 53. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 Maintenance Menu

To access this menu, select Maintenance on the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

The menu shown in Table 54 is for clearing Setup passwords and displaying processor information. Setup only displays this menu in configure mode. See Section 2.9.2 on page 75 for configure mode setting information.

Table 54. Maintenance Menu

Feature	Options	Description
Clear All Passwords	• **Ok (default)** • Cancel	Clears the user and supervisor passwords.
CPU Stepping Signature	No options	Displays CPU's Stepping Signature.
CPU Microcode Update Revision	No options	Displays CPU's Microcode Update Revision.

4.3 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 55 describes the Main menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 55. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Hyper-Threading Technology	Disabled **Enabled (default)**	Disables/enables Hyper-Threading Technology. This option is present only when a processor that supports Hyper-Threading Technology is installed.
Processor Speed	No options	Displays processor speed.
System Bus Speed	No options	Displays the system bus speed.
System Memory Speed	No options	Displays the system memory speed.
Cache RAM	No options	Displays the size of second-level cache.
Total Memory	No options	Displays the total amount of RAM.
Memory Mode	No options	Displays the memory mode (Dual Channel or Single Channel).
Memory Channel A Slot 0 Memory Channel A Slot 1 Memory Channel B Slot 0 Memory Channel B Slot 1	No options	Displays the amount and type of RAM in the DIMM sockets.
Language	• **English (default)** • (other language loaded on the board)	Selects the current default language used by the BIOS.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Day of week Month/day/year	Specifies the current date.

4.4 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

Table 56 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

Table 56. Advanced Menu

Feature	Options	Description
PCI Configuration	Select to display submenu	Configures individual PCI slot's IRQ priority.
Boot Configuration	Select to display submenu	Configures Plug and Play and the Numlock key, and resets configuration data.
Peripheral Configuration	Select to display submenu	Configures peripheral ports and devices.
Drive Configuration	Select to display submenu	Specifies type of connected IDE devices.
Floppy Configuration	Select to display submenu	Configures the diskette drive.
Event Log Configuration	Select to display submenu	Configures Event Logging.
Video Configuration	Select to display submenu	Configures video features.
USB Configuration	Select to display submenu	Configures USB support
Chipset Configuration	Select to display submenu	Configures advanced chipset features.
Fan Control Configuration	Select to display submenu	Configures fan operation.
Hardware Monitoring	Select to display submenu	Monitors system temperatures, voltages, and fan speeds

4.4.1 PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar and then PCI Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

The submenu shown in Table 57 is used to configure the IRQ priority of PCI slots individually.

Table 57. PCI Configuration Submenu

Feature	Options	Description
PCI Slot1 IRQ Priority (Note)	• **Auto (default)** • 3 • 5 • 9 • 10 • 11	Allows selection of IRQ priority for PCI bus connector 1.
PCI Slot2 IRQ Priority (Note)	• **Auto (default)** • 3 • 5 • 9 • 10 • 11	Allows selection of IRQ priority for PCI bus connector 2.
PCI Slot3 IRQ Priority (Note)	• **Auto (default)** • 3 • 5 • 9 • 10 • 11	Allows selection of IRQ priority for PCI bus connector 3.
PCI Slot4 IRQ Priority (Note)	• **Auto (default)** • 3 • 5 • 9 • 10 • 11	Allows selection of IRQ priority for PCI bus connector 4.

continued

Table 57. PCI Configuration Submenu (continued)

Feature	Options	Description
PCI Slot5 IRQ Priority (Note)	• **Auto (default)** • 3 • 5 • 9 • 10 • 11	Allows selection of IRQ priority for PCI bus connector 5.

Note: Additional interrupts may be available if certain onboard devices (such as the serial and parallel ports) are disabled.

4.4.2 Boot Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Boot Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

The submenu represented by Table 58 is for setting Plug and Play options and the power-on state of the Numlock key.

Table 58. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if manual configuration is desired. *No* lets the BIOS configure all devices. This setting is appropriate when using a Plug and Play operating system. *Yes* lets the operating system configure Plug and Play devices not required to boot the system. This option is available for use during lab testing.
Numlock	• Off • **On (default)**	Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard.

4.4.3 Peripheral Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Peripheral Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

The submenu represented in Table 59 is used for configuring computer peripherals.

Table 59. Peripheral Configuration Submenu

Feature	Options	Description
Serial Port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address (This feature is present only when Serial Port A is set to *Enabled*)	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for serial port A, if serial port A is set to *Enabled*.
Interrupt (This feature is present only when Serial Port A is set to *Enabled*)	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for serial port A, if serial port A is set to *Enabled*.

continued

Table 59. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. *Output Only* operates in AT*-compatible mode. *Bi-directional* operates in PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address (This feature is present only when Parallel Port is set to *Enabled*)	• **378 (default)** • 278	Specifies the base I/O address for the parallel port.
Interrupt (This feature is present only when Parallel Port is set to *Enabled*)	• IRQ 5 • **IRQ 7 (default)**	Specifies the interrupt for the parallel port.
DMA (This feature is present only when Parallel Port Mode is set to *ECP*)	• 1 • **3 (default)**	Specifies the DMA channel.
Audio	• **Enabled (default)** • Disabled	Enables or disables the onboard audio subsystem.
Onboard LAN	• **Enabled (default)** • Disabled	Enables or disables the onboard LAN device.

4.4.4 Drive Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Drive Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

The menu represented in Table 60 is used to configure IDE device options.

Table 60. Drive Configuration Submenu

Feature	Options	Description
ATA/IDE Configuration	• Disabled • Legacy • **Enhanced (default)**	Disabled = All IDE resources disabled Legacy = Up to two IDE channels enabled for operating systems that require legacy IDE operation Enhanced = All Serial ATA (SATA) and Parallel ATA (PATA) resources enabled
Legacy IDE Channels	• PATA Pri Only • PATA Sec Only • PATA Pri and Sec • SATA P0/P1 only • SATA P0/P1, PATA Sec • SATA P0/P1, PATA Pri	Configures PATA and SATA resources for operating systems that require legacy IDE operation. PATA = Parallel ATA SATA = Serial ATA Pri = Primary Sec = Secondary P0 = Serial ATA connector 0 P1 = Serial ATA connector 1 This feature is present only when the ATA/IDE configuration option is set to Legacy.
PCI IDE Bus Master	• Disabled • **Enabled (default)**	Enables/disables the use of DMA for hard drive BIOS INT13 reads and writes.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.

continued

Table 60. Drive Configuration Submenu (continued)

Feature	Options	Description
Soft RAID Support	• **Disabled (default)** • Enabled	Enables/disables RAID support
SATA Port-0	Select to display submenu	Reports type of device attached to Serial ATA (SATA) connector 0.
SATA Port-1	Select to display submenu	Reports type of device attached to Serial ATA (SATA) connector 1.
PATA Primary Master	Select to display submenu	Reports type of connected device on Parallel ATA (PATA) IDE primary master interface.
PATA Primary Slave	Select to display submenu	Reports type of connected device on Parallel ATA (PATA) IDE primary slave interface.
PATA Secondary Master	Select to display submenu	Reports type of connected device on Parallel ATA (PATA) IDE secondary master interface.
PATA Secondary Slave	Select to display submenu	Reports type of connected device on Parallel ATA (PATA) IDE secondary slave interface.

4.4.4.1 SATA/PATA Submenus

To access these submenus, select Advanced on the menu bar, then Drive Configuration, and then the device to be configured.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration **SATA Port-0** **SATA Port-1** **PATA Primary Master** **PATA Primary Slave** **PATA Secondary Master** **PATA Secondary Slave**
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

There are six SATA/PATA submenus: SATA Port-0, SATA Port-1, PATA primary master, PATA primary slave, PATA secondary master, and PATA secondary slave. Table 61 on page 106 shows the format of the SATA/PATA submenus. For brevity, only one example is shown.

Table 61. SATA/PATA Submenus

Feature	Options	Description
Drive Installed	No options	Displays the type of drive installed.
Type	• **Auto (default)** • User	Specifies the IDE configuration mode for IDE devices. *User* allows capabilities to be changed. *Auto* fills-in capabilities from ATA/ATAPI device.
Maximum Capacity	No options	Displays the drive capacity.
LBA/Large Mode	• Disabled • **Auto (default)**	Displays whether automatic translation mode is enabled for the hard disk. (This item is read-only unless Type is set to *User*.)
Block Mode	• Disabled • **Auto (default)**	Displays whether automatic multiple sector data transfers are enabled. (This item is read-only unless Type is set to *User*.)
PIO Mode	**Auto (default)** 0 1 2 3 4	Sets the PIO mode. (This item is read-only unless Type is set to *User*.)
DMA Mode	• **Auto (default)** • SWDMA0 • SWDMA1 • SWDMA2 • MWDMA0 • MWDMA1 • MWDMA2 • UDMA0 • UDMA1 • UDMA2	Specifies the DMA mode for the drive. *Auto* = Auto-detected *SWDMAn* = Single Word DMA*n* *SWDMAn* = Multi Word DMA*n* *UDMAn* = Ultra DMA*n* (This item is read-only unless Type is set to *User*.)
S.M.A.R.T.	• **Auto (default)** • Disabled • Enabled	Enables/disables S.M.A.R.T. (Self-Monitoring, Analysis, and Reporting Technology). (This item is read-only unless Type is set to *User*.)
Cable Detected	No options	Displays the type of cable connected to the Parallel ATA IDE interface: 40-conductor or 80-conductor (for ATA-100 peripherals).

Note: If an LS-120 drive is attached to the system, a row entitled ARMD Emulation Type will be displayed in the above table. The BIOS will always recognize the drive as an ATAPI floppy drive. The ARMD Emulation Type should always be set to Floppy.

4.4.5 Floppy Configuration Submenu

To access this menu, select Advanced on the menu bar and then Floppy Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

The submenu represented by Table 62 is used for configuring the diskette drive.

Table 62. Floppy Configuration Submenu

Feature	Options	Description
Diskette Controller	• Disabled • **Enabled (default)**	Disables or enables the integrated diskette controller.
Floppy A	• Disabled • 360 KB 5¼” • 1.2 MB 5¼” • 720 KB 3½” • **1.44 MB 3½” (default)** • 2.88 MB 3½”	Specifies the capacity and physical size of diskette drive A.
Diskette Write Protect	• **Disabled (default)** • Enabled	Disables or enables write protection for the diskette drive.

4.4.6 Event Log Configuration Submenu

To access this menu, select Advanced on the menu bar and then Event Log Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

The submenu represented by Table 63 is used to configure the event logging features.

Table 63. Event Log Configuration Submenu

Feature	Options	Description
Event Log	No options	Indicates if there is space available in the event log.
View Event Log	[Enter]	Displays the event log.
Clear Event Log	• **Ok (default)** • Cancel	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables/disables logging of DMI events.
Mark Events As Read	• **Ok (default)** • Cancel	Marks all events as read.

4.4.7 Video Configuration Submenu

To access this menu, select Advanced on the menu bar and then Video Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

The submenu represented in Table 64 is for configuring the video features.

Table 64. Video Configuration Submenu

Feature	Options	Description
AGP Aperture Size	• 4 MB • 8 MB • 16 MB • 32 MB • **64 MB (default)** • 128 MB • 256 MB	Sets the aperture size for the video controller.
Primary Video Adapter	• **AGP (default)** • PCI	Selects primary video adapter to be used during boot.

4.4.8 USB Configuration Submenu

To access this menu, select Advanced on the menu bar and then USB Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

The submenu represented in Table 65 is for configuring the USB features.

Table 65. USB Configuration Submenu

Feature	Options	Description
High-Speed USB	• **Enabled (default)** • Disabled	Set to *Disabled* when a USB 2.0 driver is not available.
Legacy USB Support	• Disabled • **Enabled (default)**	Enables/disables legacy USB support.
USB 2.0 Legacy Support	• **FullSpeed (default)** • HiSpeed	Configures the USB 2.0 Legacy support. HiSpeed = 480 Mbits/sec FullSpeed = 12 Mbits/sec

4.4.9 Chipset Configuration Submenu

To access this menu, select Advanced on the menu bar and then Chipset Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

The submenu represented in Table 66 is for configuring chipset options.

Table 66. Chipset Configuration Submenu

Feature	Options	Description
ISA Enable Bit	• Disabled • **Enabled (default)**	When set to *Enable*, a PCI-to-PCI bridge will only recognize I/O addresses that do not alias to an ISA range (within the bridge's assigned I/O range).
PCI Latency Timer	• **32 (default)** • 64 • 96 • 128 • 160 • 192 • 224 • 248	Allows you to control the time (in PCI bus clock cycles) that an agent on the PC bus can hold the bus when another agent has requested the bus.
Burn-In Mode	Select to display Burn-In mode submenu	Submenu used to set Burn-In mode configuration options.

continued

Table 66. Chipset Configuration Submenu (continued)

Feature	Options	Description
Extended Configuration	• **Default (default)** • User Defined	Allows the setting of extended configuration options.
SDRAM Frequency (Note 1)	• **Auto (default)** • 266 MHz • 333 MHz (Note 2) • 400 MHz (Note 3)	Allows override of the detected memory frequency. NOTE: If SDRAM Frequency is changed, you must reboot for the change to take effect. After changing this setting and rebooting, the System Memory Speed parameter in the Main menu will reflect the new value.
CPC Override	• **Auto (default)** • Enabled • Disabled	Controls the CPC/1n rule mode. *Enabled* allows the DRAM controller to attempt chip select assertions in two consecutive common clocks.
SDRAM Timing Control (Note 1)	• **Auto (default)** • Manual – Aggressive • Manual – User Defined	*Auto* = Timings will be programmed according to the memory detected. *Manual – Aggressive* = Selects most aggressive user-defined timings. *Manual – User Defined* = Allows manual override of detected SDRAM settings.
SDRAM RAS Active to Precharge (Note 4)	• 8 • 7 • **6 (default)** • 5	Corresponds to tRAS.
SDRAM CAS# Latency (Note 4)	• 2.0 • **2.5 (default)** • 3.0	Selects the number of clock cycles required to address a column in memory.
SDRAM RAS# to CAS# Delay (Note 4)	• 4 • **3 (default)** • 2	Selects the number of clock cycles between addressing a row and addressing a column.
SDRAM RAS# Precharge (Note 4)	• 4 • **3 (default)** • 2	Selects the length of time required before accessing a new row.

Notes:

1. This feature is displayed only if Extended Configuration is set to User Defined.
2. This option is displayed only if the installed processor has a 533 MHz system bus.
3. This option is displayed only if the installed processor has an 800 MHz system bus.
4. This feature is displayed only if SDRAM Timing Control is set to Manual – User Defined.

4.4.9.1 Burn-In Mode Submenu

To access this menu, select Advanced on the menu bar, then Chipset Configuration, and then Burn-In Mode.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration **Burn-In Mode**
Fan Control Configuration
Hardware Monitoring

The submenu represented in Table 67 is for configuring Burn-In Mode options.

Table 67. Burn-In Mode Submenu

Feature	Options	Description
Do you wish to continue?	• **No (default)** • Continue	Enables or disables setting of burn-in mode options. Burn-in Mode is an unsupported capability for use by system engineers and technicians for validation and test purposes.
Host and I/O Burn-In Mode	• **Default (default)** • –2.0% • –1.0% • +1.0% • +2.0% • +3.0% • +4.0%	Alters the host clock (system bus) and I/O clocks (AGP and PCI) by the percentage selected. If this option is set to anything other than *Default*, the AGP/PCI Burn-In Mode (shown below) is automatically set to *Default*.
AGP/PCI Burn-In Mode	• **Default (default)** • 63.88/31.94 MHz • 68.05/34.02 MHz • 69.44/34.72 MHz • 70.83/35.41 MHz • 72.22/36.11 MHz • 73.60/36.80 MHz	Enables the selection of specific AGP/PCI clock frequencies. The host clock (system bus speed) is not changed. If this option is set to anything other than *Default*, the Host and I/O Burn-In Mode (shown above) is automatically set to *Default*.

⚠ **CAUTION**

These settings are intended for validation and test purposes only. Altering host and I/O clock frequencies may reduce system stability and/or shorten the useful life of the processor. Operation at settings beyond component specification is not covered by Intel component warranties. If any problems occur during operation at non-default settings, return the board to default values.

4.4.10 Fan Control Configuration Submenu

To access this menu, select Advanced on the menu bar and then Fan Control Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

The submenu represented in Table 68 is for configuring fan control options.

Table 68. Fan Control Configuration Submenu

Feature	Options	Description
Fan Control	• Disabled • **Enabled (default)**	Enables or disables fan control.
Lowest Fan Speed	• **Slow (default)** • Off	Defines the lower limit of chassis fan speed operation. When set to *Slow*, at low system temperatures the fans will continue to run at slow speed. When set to *Off*, at low system temperatures the fans will turn off.

Note: These options will not take effect until power has been completely removed from the system. After saving the BIOS settings and turning off the system, unplug the power cord from the system and wait at least 30 seconds before reapplying power and turning the system back on.

4.4.11 Hardware Monitoring

To access this screen, select Advanced on the menu bar and then Hardware Monitoring.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
Drive Configuration
Floppy Configuration
Event Log Configuration
Video Configuration
USB Configuration
Chipset Configuration
Fan Control Configuration
Hardware Monitoring

Table 69 represents an example of the hardware monitoring display.

Table 69. Hardware Monitoring Display

Feature	Description
Processor Zone Temperature	Displays temperature in Celsius and Fahrenheit
System Zone 1 Temperature	Displays temperature in Celsius and Fahrenheit
System Zone 2 Temperature	Displays temperature in Celsius and Fahrenheit
Processor Fan Speed	Displays fan speed in RPM
Front Fan Speed	Displays fan speed in RPM
Rear Fan Speed	Displays fan speed in RPM
+1.5 V in	Displays voltage level of +1.5 V in supply
Vccp	Displays voltage level of Vccp supply
+3.3 V in	Displays voltage level of +3.3 V in supply
+5 V in	Displays voltage level of +5 V in supply
+12 V in	Displays voltage level of +12 V in supply

4.5 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented by Table 70 is for setting passwords and security features.

Table 70. Security Menu

If no password entered previously:		
Feature	**Options**	**Description**
Supervisor Password	No options	Reports if there is a supervisor password set.
User Password	No options	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters. (Note 1)	Specifies the supervisor password.
User Access Level (Note 2)	• No Access • View Only • Limited • **Full (default)**	Sets the user access rights to the BIOS Setup Utility. *No Access* prevents user access to the BIOS Setup Utility. *View Only* allows the user to view but not change the BIOS Setup Utility fields. *Limited* allows the user to changes some fields. *Full* allows the user to changes all fields except the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters. (Note 1)	Specifies the user password.
Clear User Password (Note 3)	• **Ok (default)** • Cancel	Clears the user password.
Chassis Intrusion	• **Disabled (default)** • Log • Log, notify once • Log, notify til cleared	*Disabled* = Disables Chassis Intrusion *Log* = Logs the intrusion in the event log *Log, notify once* = Halts system during POST. User must press <F4> to continue. Intrusion flag is cleared and the event log is updated. *Log, notify til cleared* = Halts system during POST. User must enter BIOS setup Security Menu and select “Clear Chassis Intrusion Status” to clear the Chassis intrusion flag.

Notes:

1. Valid password characters are A-Z, a-z, and 0-9.
2. This feature is displayed only if a supervisor password has been set.
3. This feature is displayed only if a user password has been set.

4.6 Power Menu

To access this menu, select Power from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				ACPI		

The menu represented in Table 71 is for setting the power management features.

Table 71. Power Menu

Feature	Options	Description
ACPI	Select to display submenu	Sets the ACPI power management options.
After Power Failure	• Stay Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC power loss occurs. *Stay Off* keeps the computer powered off until the power button is pressed. *Last State* restores the computer to the power state it was in before the power loss. *Power On* boots the computer when power is restored.
Wake on PCI PME	• **Stay Off (default)** • Power On	Specifies the computer responds when system power is off and a PCI power management event occurs.

4.6.1 ACPI Submenu

To access this menu, select Power from the menu bar at the top of the screen and then ACPI.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				ACPI		

The submenu represented in Table 72 is for setting the ACPI power options.

Table 72. ACPI Submenu

Feature	Options	Description
ACPI Suspend State	• S1 State • **S3 State (default)**	S1 is the safest mode but consumes more power. S3 consumes less power, but some drivers may not support this state.
Wake on LAN* from S5	• **Stay Off (default)** • Power On	In ACPI soft-off mode only, determines how the system responds to a LAN wake-up event.

4.7 Boot Menu

To access this menu, select Boot from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The menu represented in Table 73 is used to set the boot features and the boot sequence.

Table 73. Boot Menu

Feature	Options	Description
Silent Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays OEM graphic instead of POST messages.
Add-On ROM Display Mode	• **Enabled (default)** • Disabled	Enables/disables splash screen for add-in cards.
Intel(R) Rapid BIOS Boot	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
PXE Boot to LAN	• **Disabled (default)** • Enabled	Disables/enables PXE boot from LAN. Note: When set to *Enabled*, you must reboot for the Intel Boot Agent device to be available in the Boot Device menu.
USB Boot	• Disabled • **Enabled (default)**	Disables/enables booting from USB boot devices.
Boot Device Priority	Select to display submenu	Specifies the boot sequence from the available types of boot devices.
Hard Disk Drives (Note)	Select to display submenu	Specifies the boot sequence from the available hard disk drives
Removable Devices (Note)	Select to display submenu	Specifies the boot sequence from the available removable devices.
ATAPI CD-ROM Drives (Note)	Select to display submenu	Specifies the boot sequence from the available ATAPI CD-ROM drives.

Note: This feature is displayed only if this type of device is present.

4.7.1 Boot Device Priority Submenu

To access this menu, select Boot on the menu bar and then Boot Devices Priority.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 74 is for setting boot devices priority.

Table 74. Boot Device Priority Submenu

Feature	Options	Description
1st Boot Device 2nd Boot Device 3rd Boot Device (Up to the number of attached boot devices)	• 1st Floppy Drive • *Hard Drive device ID* • *ATAPI CD-ROM device ID* • Disabled	Specifies the boot sequence according to the device type. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The default settings for the first through fourth boot devices are, respectively: • Removable Dev. • Hard Drive • ATAPI CD-ROM • Disabled

Notes:

1. This option is only available when PXE Boot to LAN is set to *Enabled* in the Boot menu.
2. The boot device identifier for Intel Boot Agent (IBA) may vary depending on the BIOS release.

4.7.2 Hard Disk Drives Submenu

To access this menu, select Boot on the menu bar and then Hard Disk Drives.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 75 is for setting hard disk drive priority.

Table 75. Hard Disk Drives Submenu

Feature	Options	Description
1st Hard Disk Drive (Note)	Dependent on installed hard drives	Specifies the boot sequence from the available hard disk drives. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to twelve hard disk drives, the maximum number of hard disk drives supported by the BIOS.

4.7.3 Removable Devices Submenu

To access this menu, select Boot on the menu bar, then Removable Devices.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 76 is for setting removable device priority.

Table 76. Removable Devices Submenu

Feature	Options	Description
1st Removable Device (Note)	Dependent on installed removable devices	Specifies the boot sequence from the available removable devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four removable devices, the maximum number of removable devices supported by the BIOS.

4.7.4 ATAPI CD-ROM Drives Submenu

To access this menu, select Boot on the menu bar and then ATAPI CD-ROM Drives.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 77 is for setting ATAPI CD-ROM drive priority.

Table 77. ATAPI CD-ROM Drives Submenu

Feature	Options	Description
1st ATAPI CDROM (Note)	Dependent on installed ATAPI CD-ROM drives	Specifies the boot sequence from the available ATAPI CD-ROM drives. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four ATAPI CD-ROM drives, the maximum number of ATAPI CD-ROM drives supported by the BIOS.

4.8 Exit Menu

To access this menu, select Exit from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 78 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 78. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
Load Optimal Defaults	Loads the optimal default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages

Table 79 lists the error messages and provides a brief description of each.

Table 79. BIOS Error Messages

Error Message	Explanation
GA20 1	An error occurred with Gate A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error	No response from diskette drive.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.
HDC Failure	Error occurred trying to access hard disk controller.

continued

Table 79. BIOS Error Messages (continued)

Error Message	Explanation
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM/CMOS/PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

✏ NOTE

The POST card must be installed in PCI bus connector 1.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 80 defines the uncompressed INIT code checkpoints, Table 81 describes the boot block recovery code checkpoints, and Table 82 lists the runtime code uncompressed in F000 shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 80. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, and do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 81. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS-120, Zip*) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 82. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 5.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power-on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 82. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 82. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power-on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.

continued

Table 82. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 83 describes the bus initialization checkpoints.

Table 83. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 84 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 84. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

Table 85 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 85. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	Onboard system devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

5.4 Speaker

A 47 Ω inductive speaker is mounted on the Desktop Board. The speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker	Figure 1, page 14

5.5 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 86). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 86. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)